PHILIPS

Data handbook

Electronic components and materials

Integrated circuits

Supplement to
Book IC11N 1986

Linear LSI

SUPPLEMENT

Signetics

Elcoma – Philips Electronic Components and Materials Division – embraces a world-wide group of companies operating under the following names:

IBRAPE
Miniwatt
Mullard
PHILIPS
RTC
signetics
VALVO

Elcoma offers you a technological partnership in developing your systems to the full. A partnership to which we can bring

- world-wide production and marketing
- know-how
- systems approach
- continuity
- broad product line
- fundamental research
- leading technologies
- applications support
- quality

LINEAR LSI

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

T1	**Tubes for r.f. heating**
T2a	**Transmitting tubes for communications, glass types**
T2b	**Transmitting tubes for communications, ceramic types**
T3	**Klystrons**
T4	**Magnetrons for microwave heating**
T5	**Cathode-ray tubes** Instrument tubes, monitor and display tubes, C.R. tubes for special applications
T6	**Geiger-Müller tubes**
T8	**Colour display systems** Colour TV picture tubes, colour data graphic display tube assemblies, deflection units
T9	**Photo and electron multipliers**
T10	**Plumbicon camera tubes and accessories**
T11	**Microwave semiconductors and components**
T12	**Vidicon and Newvicon camera tubes**
T13	**Image intensifiers and infrared detectors**
T15	**Dry reed switches**
T16	**Monochrome tubes and deflection units** Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1 **Diodes**
Small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2a **Power diodes**

S2b **Thyristors and triacs**

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Surface mounted semiconductors**

S8a **Light-emitting diodes**

S8b **Devices for optoelectronics**
Optocouplers, photosensitive diodes and transistors, infrared light-emitting diodes and infrared sensitive devices, laser and fibre-optic components

S9 **Power MOS transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

S11 **Microwave transistors**

S12 **Surface acoustic wave devices**

S13 **Semiconductor sensors**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

EXISTING SERIES		Superseded by:
IC1	**Bipolar ICs for radio and audio equipment**	IC01N
IC2	**Bipolar ICs for video equipment**	IC02Na and IC02Nb
IC3	**ICs for digital systems in radio, audio and video equipment**	IC01N, IC02Na and IC02Nb
IC4	**Digital integrated circuits** CMOS HE4000B family	
IC5	**Digital integrated circuits — ECL** ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs	IC08N
IC6	**Professional analogue integrated circuits**	IC03N and Supplement to IC11N
IC7	**Signetics bipolar memories**	
IC8	**Signetics analogue circuits**	IC11N
IC9	**Signetics TTL logic**	IC09N and IC15N
IC10	**Signetics Integrated Fuse Logic (IFL)**	IC13N
IC11	**Microprocessors, microcomputers and peripheral circuitry**	IC14N

NEW SERIES

IC01N	**Radio, audio and associated systems** Bipolar, MOS	(published 1985)
IC02Na	**Video and associated systems** Bipolar, MOS Types MAB8031AH to TDA1524A	(published 1985)
IC02Nb	**Video and associated systems** Bipolar, MOS Types TDA2501 to TEA1002	(published 1985)
IC03N	**Integrated circuits for telephony**	(published 1985)
IC04N	**HE4000B logic family** CMOS	
IC05N	**HE4000B logic family — incased ICs** CMOS	(published 1984)
IC06N*	**High-speed CMOS; PC74HC/HCT/HCU** Logic family	(published 1986)
IC07N	**High-speed CMOS; PC54/74HC/HCT/HCU — uncased ICs** Logic family	
IC08N	**ECL 10K and 100K logic families**	(published 1984)
IC09N	**TTL logic series**	(published 1984)
IC10N	**Memories** MOS, TTL, ECL	
IC11N	**Linear LSI**	(published 1985)
Supplement to IC11N	**Linear LSI**	(published 1986)
IC12N	**Semi-custom gate arrays & cell libraries** ISL, ECL, CMOS	
IC13N	**Semi-custom** Integrated Fuse Logic	(published 1985)
IC14N	**Microprocessors, microcontrollers & peripherals** Bipolar, MOS	(published 1985)
IC15N	**FAST TTL logic series**	(published 1984)

Note

Books available in the new series are shown with their date of publication.

* Supersedes the IC06N 1985 edition and the Supplement to IC06N issued Autumn 1985.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C1 **Programmable controller modules**
PLC modules, PC20 modules

C2 **Television tuners, coaxial aerial input assemblies, surface acoustic wave filters**

C3 **Loudspeakers**

C4 **Ferroxcube potcores, square cores and cross cores**

C5 **Ferroxcube for power, audio/video and accelerators**

C6 **Synchronous motors and gearboxes**

C7 **Variable capacitors**

C8 **Variable mains transformers**

C9 **Piezoelectric quartz devices**

C10 **Connectors**

C11 **Varistors, thermistors and sensors**

C12 **Potentiometers, encoders and switches**

C13 **Fixed resistors**

C14 **Electrolytic and solid capacitors**

C15 **Ceramic capacitors**

C16 **Permanent magnet materials**

C17 **Stepping motors and associated electronics**

C18 **Direct current motors**

C19 **Piezoelectric ceramics**

C20 **Wire-wound components for TVs and monitors**

C21* **Assemblies for industrial use**
HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices

C22 **Film capacitors**

* To be issued shortly.

PREFACE

The linear LSI Division, one of five Signetics divisions, is a major supplier of a broad line of linear integrated circuits ranging from high-performance designs to many of the more popular industry standard devices and custom designs.

Employing Signatics' high quality processing and screening standards, the Linear LSI Division is dedicated to providing high quality Linear products to our world-wide customers. Our full product line addresses the needs of the EDP, Automotive, Industrial, Consumer and Communication markets.
The 1986 Supplement to our Linear LSI book of 1985 provides complete technical data on our full line of interface, communication, amplifier, power conversion and control products. Among these you will find new entrants such as the NE5205 high frequency amplifier, NE5170 and NE5180/5181 octal line driver and receivers, and the DAC800 12-bit D/A Converter.

An applications section, selector guides and cross reference guides are also included in this volume.

Although every attempt has been made to insure accuracy of information in this manual, Signetics assumes no liability for inadvertent errors.

Signetics Linear LSI Marketing

PRODUCT STATUS DEFINITIONS

DEFINITION OF TERMS

Data Sheet Identification	Product Status	Definition
Preview	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Advance Information	Sampling or Pre-Production	This data sheet contains advance information and specifications are subject to change without notice.
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains final specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

CONTENTS

* For up-to-date cross reference information contact your local sales office.

CONTENTS

CONTENTS

Section 1
Selection Guide

INDEX

SO Availability

Part Number	SMD Package	Description
*DAC08ED	SO-16	8-Bit D/A Converter
*LF398D	SO-14	Sample and Hold Amp
LM1870D	SOL-20	Stereo Demodulator
LM2901D	SO-14	Quad Volt Comparator
LM2903D	SO-8	Dual Volt Comparator
LM311D	SO-8	Voltage Comparator
LM319D	SO-14	High Speed Dual Comparator
LM324AD	SO-14	Quad Op Amp
LM324D	SO-14	Quad Op Amp
LM339D	SO-14	Quad Volt Comparator
LM358D	SO-8	Dual Op Amp
LM393D	So-8	Dual Comparator
*MC1408-8D	SO-16	8-Bit D/A Converter
MC1458D	SO-8	Dual Op Amp
MC1488D	SO-14	Quad Line Driver
MC1489AD	SO-14	Quad Line Receiver
MC1489D	SO-14	Quad Line Receiver
MC3302D	SO-14	Quad Volt Comparator
MC3403D	SO-14	Quad Low Power Op Amp
NE4558D	SO-8	Dual Op Amp
*NE5008D	SO-16	8-Bit D/A Converter
*NE5018D	SOL-24	8-Bit D/A Converter
*NE5019D	SOL-24	8-Bit D/A Converter
*NE5036D	SO-14	6-Bit A/D Converter
NE5037D	SO-16	6-Bit A/D Converter
NE5044D	SO-16	Programmable 7-Channel Encoder
NE5045D	SO-16	7-Channel Decoder
NE5090D	SOL-16	Address Relay Driver
NE5205D	SO-8	High Frequency Amp
NE521D	SO-14	High Speed Dual Comparator
NE522D	SO-14	High Speed Dual Comparator
NE5230D	SO-8	Low Voltage Op Amp
NE527D	SO-14	High Speed Comparator
NE529D	SO-14	High Speed Comparator
NE532D	SO-8	Dual Op Amp
*NE544D	SOL-16	Servo Amp
*NE5512D	SO-8	Dual High Performance Op Amp
*NE5514D	SOL-16	Quad High Performance Op Amp
NE5517D	SO-16	Dual High Performance Amp
NE5520D	SOL-16	LVDT Signal Conditioner Circuit
*NE5532D	SOL-16	Dual Low Noise Op Amp
*NE5533D	SOL-16	Low Noise Op Amp
NE5534AD	SO-8	Low Noise Op Amp
NE5534D	SO-8	Low Noise Op Amp
*NE5537D	SO-14	Sample and Hold Amp
NE5539D	SO-14	High Frequency Wideband Amp
NE555D	SO-8	Single Timer
NE556D	SO-14	Dual Timer
NE5560D	SO-16	SMPS Control Circuit
NE5561D	SO-8	SMPS Control Circuit
NE5562D	SOL-20	SMPS Control Circuit
NE5568D	SO-8	SMPS Control Circuit

**Non-standard pinout.*
(Please check 1985 Linear Data Manual for additional pinout information.)
For information regarding additional SO products released since the publication of this document, contact your local Signetics sales office.

SO Availability

Part Number	SMD Package	Description
NE558D	SOL-16	Quad Timer
NE5592D	SO-14	Dual Video Amp
NE564D	SO-16	High Frequency Phase Locked Loop
*NE565D	SO-14	Phase Locked Loop
NE566D	SO-8	Function Generator
NE567D	SO-8	Tone Decoder Phase Locked Loop
NE571D	SOL-16	Compandor
NE572D	SOL-16	Programmable Compandor
*NE587D	SOL-20	7-Segment LED Driver (Anode)
*NE589D	SOL-20	7-Segment LED Driver (Cathode)
NE592D14	SO-14	Video Amp
NE592D8	SO-8	Video Amp
NE592HD14	SO-14	High Gain Video Amp
NE592HD8	SO-8	High Gain Video Amp
*NE594D	SOL-20	Vacuum Fluorescent Display Driver
NE602D	SO-8	Double Balanced Mixer/Oscillator
NE604D	SO-16	Low Power FM IF System
NE612D	SO-8	Double Balanced Mixer/Oscillator
NE614D	SO-16	Low Power FM IF System
SA571D	SOL-16	Compandor
SA572D	SOL-16	Compandor
*SA594D	SOL-20	Vacuum Fluorescent Display Driver
SA602D	SO-8	Double Balanced Mixer/Oscillator
SA604D	SO-16	Low Power FM IF System
SG3524D	SO-16	SMPS Control Circuit
ULN2003D	SO-16	Transistor Array
ULN2004D	SO-16	Transistor Array
μA723CD	SO-14	Voltage Regulator
μA741CD	SO-8	Single Op Amp
μA747CD	SO-14	Dual Op Amp

**Non-standard pinout.*

For information regarding additional SO products released since the publication of this document, contact your local Signetics sales office.

Ordering Information

FOR PREFIXES AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

ORDERING INFORMATION

Signetics' Linear LSI integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:
- $1000 per order
- $250 per line item per order

Military Product:
- $250 per line item per order

Table 1 provides part number information concerning Signetics originated products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Tables 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted, however, that devices with a SE prefix (−55°C to +125°C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any Linear LSI product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

Table 1 PART NUMBER DESCRIPTION

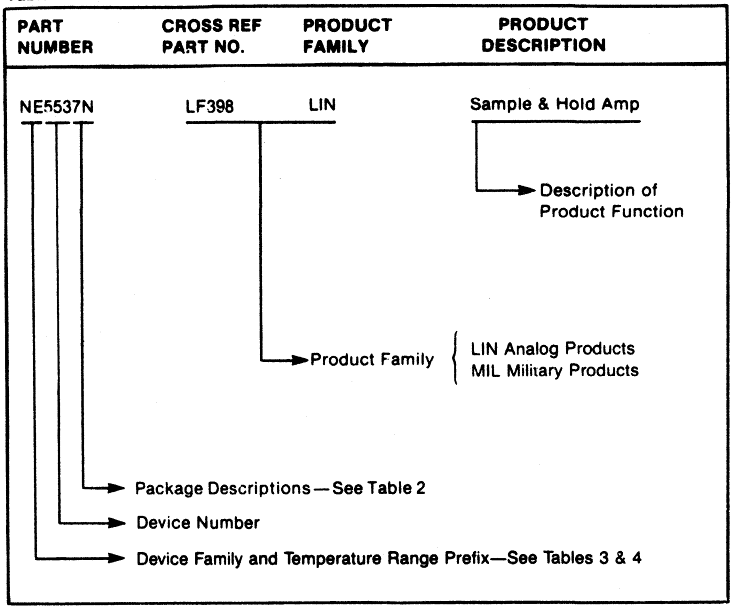


Table 2 PACKAGE DESCRIPTIONS

Old	New	PACKAGE DESCRIPTION
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
-	D	Microminiature package (SO)
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
T,TA	H	8-lead TO-99
U	U	SIL Plastic power
V	N	8-lead plastic DIL
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 3 SIGNETICS PREFIX AND DEVICE TEMPERATURE

PREFIX	DEVICE TEMPERATURE RANGE
N	0° to +70°C
S	−55° to +125°C
NE	0° to +70°C
SE	−55° to +125°C
SA	−40° to +85°C

Table 4 INDUSTRY STANDARD PREFIX

PREFIX	DEVICE FAMILY
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
JB	Mil Rel—Jan Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LF	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
NE	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
ULN	Linear Industry Standard

Section 2
Quality and Reliability

INDEX

Quality and Reliability

SIGNETICS LINEAR QUALITY

Signetics has put together a winning process for manufacturing linear circuits. Our standard is zero defects, and current customer quality statistics demonstrate our commitment to this goal.

The circuits produced in the Linear Division must meet rigid criteria as defined by our design rules and as evaluated with a thorough product characterization and quality process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide QA05 data base system. The SURE (Systematic Uniform Reliability Evaluation) program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent product-related problems and to inform our customers and employees of our progress in achieving zero defects.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 5 x 10(fifth) amps/cm(sq). Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same ground potential, thereby precluding internal noise problems.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to insure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees.

QUALIFICATION

Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

QA05 – QUALITY DATA BASE REPORTING SYSTEM

The QA05 data reporting system collects the results of product assurance testing on all finished lots and feeds this data back to concerned organizations where appropriate action can be taken. The QA05 reports EPQ (Estimated Process Quality) and AOQ (Average Outgoing Quality) results for electrical, visual/mechanical, hermeticity, and documentation audits. Data from this system is available on request.

THE SURE PROGRAM

The SURE (Systematic Uniform Reliability Evaluation) program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE program has two major functions: Long-term accelerated stress performance audit and a short-term accelerated stress monitor. Samples are selected that represent all generic product groups in all wafer fabrication and assembly locations.

THE LONG-TERM AUDIT

One-hundred devices from each generic family are subjected to each of the following stresses every four weeks:

- **High Temperature Operating Life: Tj = 150°C, 1000 hours, static biased operation.**
- **High Temperature Storage: Tj = 150°C, 1000 hours**
- **Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static biased**

THE SHORT-TERM MONITOR

Every other week a 50-piece sample from each generic family is run to 72 hours of pressure pot (20psig, 127°C, 100% saturated steam) and 300 cycles of thermal shock (−65°C to +150°C)

In addition, each Signetics assembly plant performs SURE product monitor stresses weekly on each generic family and molded package by pin count and frame type. Fifty-piece samples are run on each stress, pressure pot to 96 hours, thermal shock to 300 cycles.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

Quality and Reliability

RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the Linear SURE program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractors.
- Device or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in some evaluation programs.

FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

ZERO DEFECTS PROGRAM

In recent years, United States industry has increasingly demanded improved product quality. We at Signetics believe that the customer has every right to expect quality products from a supplier. The benefits which are derived from quality products can be summed up in the words, *lower cost of ownership.*

Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times and more rework.

SIGNETICS UNDERSTANDS CUSTOMERS' NEEDS

Signetics has long had an organization of quality professionals, inside all operating units, coordinated by a corporate quality department. This broad decentralized organization provides leadership, feedback, and direction for achieving a high level of quality. Special programs are targeted on specific quality issues. For example, in 1978 a program to reduce electrically defective units for a major automotive manufacturer improved outgoing quality levels by an order of magnitude.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100PPM (parts per million), down from an industry practice of 10,000PPM, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented low defect levels could only be achieved by contributions from all employees, from the R and D laboratory to the shipping dock. In short, from a program that would effect a total cultural change within Signetics in our attitude toward quality.

QUALITY PAYS OFF FOR OUR CUSTOMERS

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold since 1980. Today, many major customers no longer test Signetics circuits. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Other customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers report a significant improvement in overall quality (see Figure 1).

At Signetics, quality means more than working circuits. It means on-time delivery of the right product at the agreed upon price (see Figure 2).

ONGOING QUALITY PROGRAM

The Signetics quality improvement program steers its employees toward "Doing it Right the First Time." The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared by all technical and administrative functions equally.

This program extends into every area of the company, and more than 40 quality improvement teams throughout the organization drive its ongoing refinement and progress.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is the cost of quality.

QUALITY COLLEGE

Almost continuously in session, Quality College is a prerequisite for all employees. The intensive curriculum is built around the four absolutes of quality; colleges are conducted at company facilities throughout the world.

"MAKING CERTAIN" – ADMINISTRATIVE QUALITY IMPROVEMENT

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for the prevention of errors.

CORRECTIVE ACTION TEAMS

Employees with the perspective, knowledge, and necessary skills to solve a problem are formed into ad hoc groups called Corrective Action Teams. These teams, a major force within the company for quality improvement, resolve administrative, technical and manufacturing problems.

Quality and Reliability

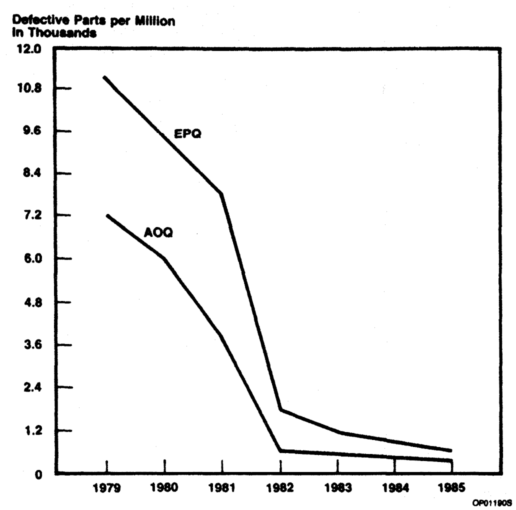


Figure 1. Signetics' Quality Progress – Estimated Process Quality and Average Outgoing Quality

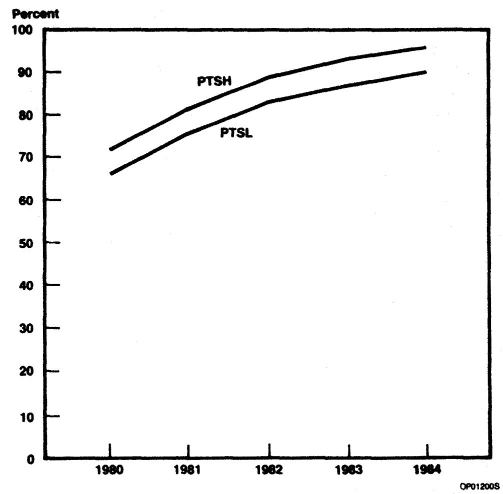


Figure 2. Performance To Schedule/On-Time Delivery – High and Low

ECR SYSTEM (ERROR CAUSE REMOVAL)

The ECR System permits employees to report to management any impediments to doing the job right the first time. Once such an impediment is reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through defect prevention.

PRODUCT QUALITY PROGRAM

To reduce defects in outgoing products, we created the Product Quality Program. This is managed by the Product Engineering Council, composed of the top product engineering and test professionals in the company. This group:

1. sets aggressive product quality improvement goals;
2. provides corporate-level visibility and focus on problem areas;
3. serves as a corporate resource for any group requiring assistance in quality improvement; and
4. drives quality improvement projects.

As a result of this aggressive program, every major customer who reports back to us on product performance is reporting significant progress.

VENDOR CERTIFICATION PROGRAM

Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent. Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in Figure 3. Simultaneously, waivers of incoming material have been eliminated.

Higher incoming quality material to us ensures higher outgoing quality products.

QUALITY AND RELIABILITY ORGANIZATION

Quality and reliability professionals at the divisional level are involved with all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions

- Manufacturing quality control
- Product assurance testing
- Laboratory facilities – failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

COMMUNICATING WITH EACH OTHER

For information on Signetics' quality programs or for any question concerning product quality, the field salesperson in your area will provide you with the quickest access to answers.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. Here are some ways we can help each other:

- Provide us with one informed contact within your organization. This will

Quality and Reliability

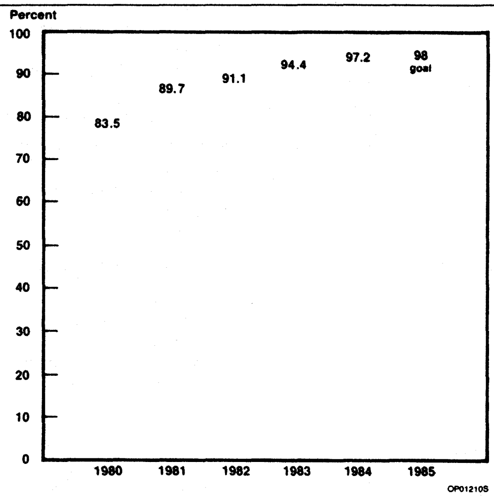


Figure 3. Lot Acceptance Rate From Signetics Vendors

MATERIAL WAIVERS

1985 – (0) (Goal)
1984 – 0
1983 – 0
1982 – 2
1981 – 134

establish continuity and build confidence levels.

- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur.
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance.
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action.
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

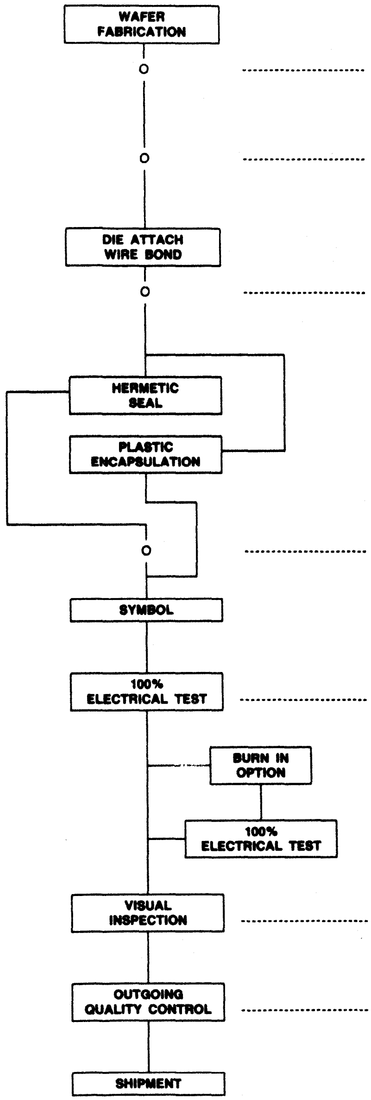
This team work with you will allow us to achieve our mutual goal of improved product quality.

MANUFACTURING: DOING IT RIGHT THE FIRST TIME

In dealing with the standard manufacturing flows, it was recognized that significant improvement would be achieved by "doing every job right the first time," a key concept of the quality improvement program. During the development of the program many profound changes were made. Figure 4, *Linear Flow*, shows the results.

The achievements resulting from the improved process flow have helped Signetics to be recognized as the leading Quality supplier of linear circuits. These achievements have also led to our participation in many Ship-to-Stock programs, which our customers use to eliminate incoming inspection. Such programs reduce the user *cost of ownership* by saving both time and money.

Quality and Reliability



SCANNING ELECTRON MICROSCOPE CONTROL

Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE

Product is inspected for defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Defects such as scratches, smears and glassivated bonding pads are included in the lot acceptance criteria.

PRE-SEAL VISUAL ACCEPTANCE

Product is inspected to detect any damage incurred at the die attach and wire bonding stations. Defects such as scratches, contamination and smeared ball bonds are included in the lot acceptance criteria.

SEAL TESTS

Hermetic package seal integrity is ensured by fine 100% gross leak testing.

SYMBOL

Devices are marked with the Signetics logo, device number and date code or custom symbol per individual specification requirements.

100% PRODUCTION ELECTRICAL TESTING

Every device is tested to all data sheet parameters guaranteeing temperature specifications.

BURN IN (SUPR II LEVEL B OPTION)

Devices are burned in for 21 hours at 155°C maximum Junction Temperature.

100% PRODUCTION ELECTRICAL TESTING

Every device is tested to all data sheet parameters guaranteeing temperature specifications.

VISUAL

All products are 100% visually inspected per the requirements specified in Signetics' or customer documents.

FINAL QUALITY ASSURANCE GATE

The final QA inspection step guarantees the specified mechanical and electrical AQL's. Every shipment is sealed and identified by QA personnel.

Figure 4. Linear Division Linear Process Flow

Quality and Reliability

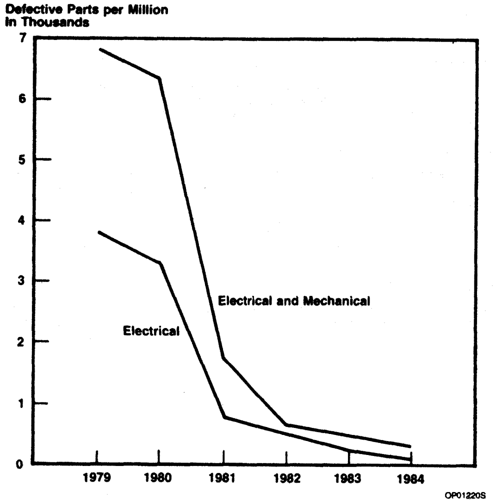


Figure 5. Linear AOQ Average Outgoing Quality

Section 3
Military

INDEX

Military Errata

Effective January 1, 1985, this section has been superseded by the 1985 Military Products Data Manual. Information regarding this manual can be obtained from the Military Division in Sacramento. (916) 925-6700.
Electrical specification herein as described for products with the "SE" prefix do not necessarily describe the performance characterization of military processed products.

Section 4
Interface Data Conversion Products

INDEX

D/A and A/D Converter—Symbols and Definitions

Absolute Accuracy Error

Absolute Accuracy Error is the difference between the theoretical analog input required to produce a given output code and the actual analog input required to produce the same code. The actual input is a range and the error is the midpoint of the measured band and the theoretical band.

Absolute Maximum Ratings

The Absolute Maximum Ratings are the operating safe zones. Exceeding these limits could cause permanent damage to the device. The device is NOT guaranteed to operate at these limits.

Conversion Speed

Conversion Speed is the speed at which a converter can make repetitive conversions.

Conversion Time

Conversion time is the time required for a complete conversion cycle of an ADC. Conversion time is a function of the number of bits and the clock frequency.

Differential Non-Linearity (DNL)

Differential Non-Linearity of a DAC is the deviation of the measured output step size from the ideal step size. In an ADC it is the deviation in the range of inputs from 1 LSB that causes the output to change from one given code to the next code. Excessive DNL gives rise to non-monotonic behavior in a DAC and missing codes in an ADC.

Differential Non-Linearity Tempco

Differential Non-Linearity Tempco is the temperature coefficient of DNL and specifies how DNL changes with temperature.

Full Scale Tempco

Full Scale Tempco in a DAC is the change of full scale output with a change of temperature. In an ADC it is the change in the input required to cause full scale transistion. Expressed in ppm/degree C.

Gain Error

Gain Error is the error of the slope of the line drawn through the midpoints of the steps of the transfer function as compared to the ideal slope. It is usually measured by determining the error of the analog input voltage to cause a full scale output word with the ideal value that should cause this full scale output. This gain error is usually expressed in LSB or in percent of full scale range.

Hysteresis Error

Hysteresis Error is the code transition voltage dependence relative to the direction from which the transistion is approached.

Integral Non-Linearity

Integral Non-Linearity is the difference between the ideal transfer characteristic and the actual characteristic.

Least Significant Bit (LSB)

The Least Significant Bit is the lowest order bit, or the bit with the least weight.

Missing Code

A Missing Code is a code combination that does not appear in the ADC's output range.

Monotonicity

A DAC is monotonic if its output either increases or remains the same when the input code is incremented from any code to the next higher code.

Most Significant Bit (MSB)

The Most Significant Bit is the highest order bit, or the one with the most weight.

Offset Error

Offset error is the constant error or shift from the ideal transfer characteristic of a converter. In a DAC it is the output obtained when that output should be zero. In an ADC it is the difference between the input level that causes the first code transistion and what that input level should be.

Output Voltage Compliance

Output Voltage Compliance of a current output DAC is the range of acceptable voltages at the DAC output for the DAC output current to remain within its specified limits.

Power Supply Sensitivity

Power Supply Sensitivity of a DAC is the change of output current or voltage with changes in the power supply voltage. In an ADC, it is the change in the transistion points from code to code with changes in the power supply voltage.

Quantizing Error

In an A/D converter there is an infinite number of possible input levels, but only 2^n output codes (n = number of bits). There will, therefore, be an error in the output code that could be as great as ½ LSB because of this quantizing effect. The greatest error occurs at the transistion point where the output state changes.

Relative Accuracy

Relative Accuracy is a measure of the difference of the theoretical output value with a given input after any offset and gain errors have been nulled out.

Resolution

Resolution is the number of bits at the input or output of an ADC or DAC. It is the number of discrete steps or states at the output and is equal to 2^n where in is the resolution of the converter. However, n bits of resolution does not guarantee n bits of accuracy.

Setting Time

Setting Time is the delay in a DAC from the 50 percent point on the change in the input digital code to the effected change in the output signal. It is expressed in terms of how long it takes the output to settle to and remain within a certain error band around the final value and is usually specific for full scale range changes.

Transfer Characteristic

The Transfer Characteristic is the relationship of the output to the input.

NOTE:
Refer to Section 9 (Interface Circuits) for an in-depth explanation of data converters and their applications.

4

Converter Selector Guides

D/A CONVERTERS

DEVICE	BITS	ACC. %	CONV. SPEED (μs)	OUTPUT V	OUTPUT I	INT. REF.	INT. LATCH	PACKAGE N	PACKAGE D	PACKAGE F	TEMPERATURE RANGE Com'l.	TEMPERATURE RANGE Mil	COMMENTS
MC1408-7	8	0.39	0.07		X			X		X			
MC1408-8	8	0.19	0.07		X			X	X	X	X		
MC1508-8	8	0.19	0.07		X					X		X	
DAC08	8	0.19	0.07		X					X		X	
DAC08A	8	0.10	0.07		X					X		X	
DAC08C	8	0.39	0.07		X			X		X	X		
DAC08E	8	0.19	0.07		X			X	X	X	X		
DAC08H	8	0.10	0.07		X			X		X	X		
NE5018	8	0.19	0.2	X		X	X	X		X	X		
SE5018	8	0.19	0.2	X		X	X			X		X	
NE5019	8	0.10	0.2	X		X	X	X		X	X		
SE5019	8	0.10	0.2	X		X	X			X			
NE5118	8	0.19	2.3		X	X	X	X		X	X		
SE5118	8	0.19	2.3		X	X	X			X		X	
NE5119	8	0.10	2.3		X	X	X	X		X	X		
SE5119	8	0.10	2.3		X	X	X			X		X	
NE5020	10	0.10	5.0	X		X	X	X		X	X		
NE5410	10	0.05	0.25		X					X	X		±¼ LSB DNL
SE5410	10	0.05	0.25		X					X		X	±¼ LSB DNL
MC3410	10	0.05	0.25		X					X	X		±½ LSB DNL
MC3510	10	0.05	0.25		X					X		X	±½ LSB DNL
AM6012	12	0.05	0.25		X					X	X		±1 LSB DNL

A/D CONVERTERS

DEVICE	BITS	ACC.%	CONV. SPEED (μs)	INPUT V	INPUT I	THREE-STATE OUTPUT	INT. REF.	INT. CLOCK	PACKAGE N	PACKAGE F	PACKAGE FE	TEMPERATURE RANGE Com'l.	TEMPERATURE RANGE Mil
NE5034	8	0.19	17		X	X		X		X		X	
NE5036	6	0.78	23	X		X			X		X	X	
NE5037	6	0.78	9	X		X			X	X		X	
ADC0801-1	8	0.10	73	X		X		X		X		X[1]	
ADC0802-1	8	0.19	73	X		X		X		X		X[1]	
ADC0803-1	8	0.19	73	X		X		X		X		X[1]	
ADC0804-1	8	0.39	73	X		X		X		X		X[1]	
ADC0805-1	8	0.39	73	X		X	X	X		X		X[1]	

Note:

1. **Automotive temperature range: – 40 to + 85°C**

10-Bit High Speed Microprocessor-Compatible Analog to Digital Converter

SE/NE5030

DESCRIPTION

The SE/NE5030 is a monolithic 10-bit, microprocessor compatible Analog-to-Digital Converter which is manufactured on a high speed bipolar process using thin film resistors. The conversion process is a new multi-step technique which combines parallel conversion and successive approximation, allowing complete 10-bit conversion in just 2.5 microseconds at the maximum 3MHz clock rate. The fast conversion rate makes the SE/NE5030 excellent for a wide range of applications where system throughput sampling rates up to 360KHz are required.

FEATURES

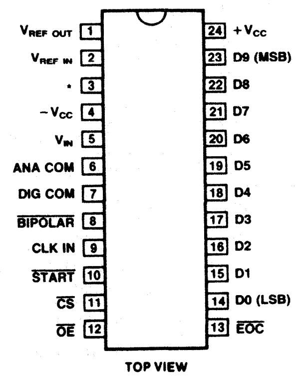
- **Microprocessor compatible**
- **Fast conversion (2.5μsec)**
- **Relative accuracy 1/4 LSB typical**
- **2.5 volt signal input range**
- **Accomodates either unipolar or bipolar input**
- **TTL compatible digital inputs/outputs**
- **No missing codes over temp range**
- **Three state outputs**
- **High impedance analog input**
- **Low TC internal reference (5ppm/°C typical)**

APPLICATIONS

- **Process control**
- **Test and measurement**
- **Machine tools**
- **Robotics**
- **Industrial monitoring**
- **High speed waveform digitizing**
- **High speed correlators**

PIN CONFIGURATION

F PACKAGE



CD01281S

* Make no external connection

ORDER NUMBERS
NE5030F, SE5030F

PIN #	DESIGNATION	FUNCTION
1	$V_{REF\ OUT}$	2.5V reference output voltage of the temperature compensated internal reference.
2	$V_{REF\ IN}$	Reference input for the converter. (Connect pin 1 to pin 2 or connect an external 2.500V reference voltage to pin 2.)
3		Make no external connection.
4	V_{EE}	−5V (±5%) negative supply pin.
5	V_{IN}	Analog input voltage. Unipolar range 0V to $+V_{REF}$; Bipolar range $-V_{REF}/2$ to $+V_{REF}/2$
6	ANA COM	Analog common point to which all Analog signals are to be referenced.
7	DIG COM	Digital common point to which all digital signals are to be referenced.
8	$\overline{BIPOLAR}$	Logic input for selecting either unipolar or bipolar mode of operation. Logic high selects unipolar mode; Logic low selects bipolar mode
9	CLOCK	Single phase clock signal input
10	$\overline{START}$	Start signal input. Low-going edge initiates a conversion cycle.
11	$\overline{CS}$	Chip Select. Must be low to enable conversion or read output data. Logic low causes normal operation (enables operation); Logic high inhibits conversion and holds output data lines in high impedance mode
12	$\overline{OE}$	Output enable. Logic low when $\overline{CS}$ is low enables output buffers; Logic high puts outputs into the high impedance state
13	$\overline{EOC}$	End of Conversion output signal. This output voltage goes low after the end of a conversion. This output voltage is reset to a logic high by a low level on the $\overline{OE}$ pin.
14-23	D0 − D9	Three-state buffer outputs (D9 is MSB, D0 is LSB). When $\overline{OE}$ is low, the converted data word is available at these pins.
24	V_{CC}	+5V (±5%) positive supply voltage pin.

4

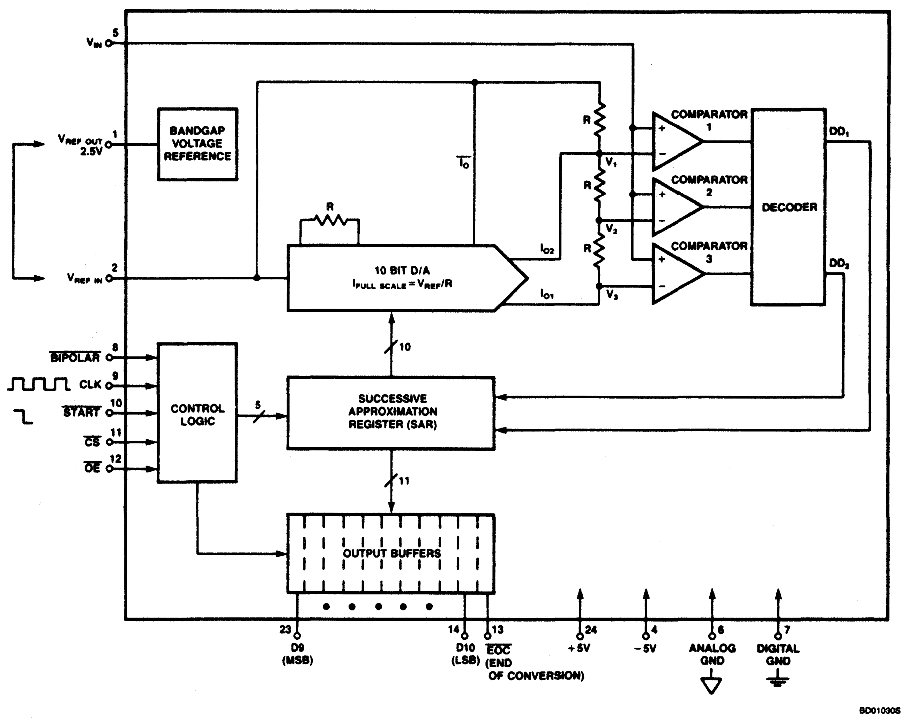
10-Bit High Speed Microprocessor-Compatible Analog to Digital Converter

SE/NE5030

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage	+8	V
Negative supply voltage	-8	V
Analog input range	±3.5	V
Digital input voltage	-0.5 to V_{CC}	V
Analog common to digital common	±1	V
$V_{REF\ OUT}$ short circuit to common	Indefinite	
$V_{REF\ OUT}$ short circuit to V_{CC}	60	seconds
$V_{REF\ IN}$ applied voltage	0 to 5	V
Digital output pins applied voltage to logic high outputs	-0.5 to V_{CC}	V
Digital output sink current	10	mA
Operating temperature range NE5030 SE5030	 0 to +70 -55 to +125	 °C °C
Storage temperature range	-60 to +150	°C
Power dissipation	600	mW

BLOCK DIAGRAM



10-Bit High Speed Microprocessor-Compatible Analog to Digital Converter

SE/NE5030

DC ELECTRICAL CHARACTERISTICS $V_{CC}=5V$, $V_{EE}=-5V$, $T_A=0$ to 70°C for NE5030, $T_A=-55$ to +125°C for SE5030, $F_{CLK} \leq 3MHz$, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Resolution		10	10	10	Bits
	Relative accuracy error[1, 2]			±1/4	±1/2	LSB
DNL	Differential linearity error[3]				10	bits
	Code width error			±1/4	±1/2	LSB
E_{FS}	Full scale gain error	$T_A=25°C$ over operating temp range		±1 ±1	±2 ±5	LSB LSB
E_{UOS}	Unipolar offset error	$T_A=25°C$ over operating temp range			±0.5 ±1.0	LSB LSB
E_{BOS}	Bipolar offset error	$T_A=25°C$ over operating temp range			±0.5 ±1.0	LSB LSB
	Analog input range Unipolar Bipolar	 $\overline{BIPOLAR}=2.0V$ $\overline{BIPOLAR}=0.8V$	 0 $-V_{REF}/2$		 $+V_{REF}$ $+V_{REF}/2$	 V V
I_B	Analog input bias current			1	5	μA
Z_{IN}	Analog input impedance		1	3		Megohms
V_{REF}	Reference voltage output	$T_A=25°C$	2.495	2.500	2.505	V
TC_{REF}	Reference voltage drift[4]	over operating temp range		±1.25 (±5)	±2.5 (±10)	mV (ppm/°C)
$I_{L\ (REF)}$	Reference external load		2	2.5		mA
$I_{REF\ IN}$	Reference input current	$V_{REF\ IN}=2.5V$		2	3	mA
V_{CC}	Pos supply operating range		4.75	5	5.25	V
V_{EE}	Neg supply operating range		-4.75	-5	-5.25	V
P_{SR}	Power supply rejection[5]	$V_{CC}=4.75$ to 5.25V $V_{EE}=-4.75$ to -5.25V			±0.25	LSB
I_{CC}	Positive supply current	$V_{CC}=5.25V$, $V_{EE}=-5.25V$		36	45	mA
I_{EE}	Negative supply current	$V_{CC}=5.25V$, $V_{EE}=-5.25V$		50	60	mA
Logic inputs						
V_{IH}	Logic 1 input voltage		2.0			V
V_{IL}	Logic 0 input voltage				0.8	V
I_{IH}	Logic 1 input current	$V_{IH}=2.4V$, $T_A=25°C$ $V_{IH}=2.4V$, over operating temp range			10 20	μA μA
I_{IL}	Logic 0 input current	$V_{IL}=0.4V$, $T_A=25°C$ $V_{IL}=0.4V$, over operating temp range			200 400	μA μA
Logic outputs						
V_{OH}	Logic 1 output voltage	$I_{OH}=-400\mu A$, $\overline{CS}=\overline{OE}=0.8V$	2.4	3.2		V
V_{OL}	Logic 0 output voltage	$I_{OL}=1.6mA$, $\overline{CS}=\overline{OE}=0.8V$		0.2	0.4	V
I_{OZ}	Three-state leakage	$\overline{OE}=2.0V$, $V_{OL}=0V$ or 5V, $T_A=25°C$ $\overline{OE}=2.0V$, $V_{OL}=0V$ or 5V, over temp		±10	±20 ±100	μA μA

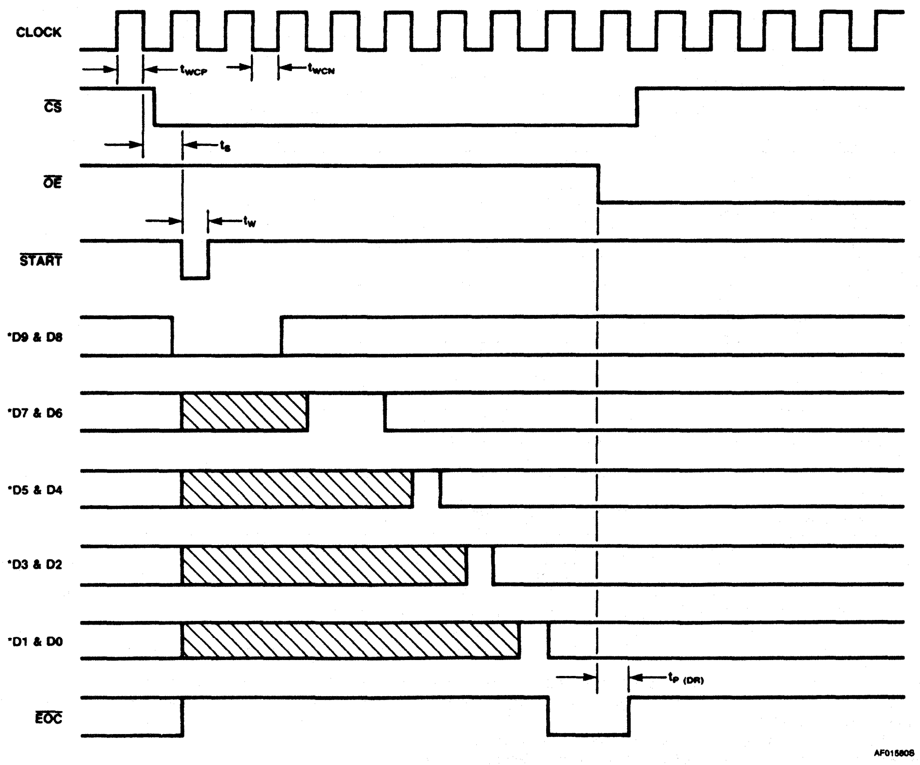
NOTES:
1. Specifications given in LSB refer to the weight of the least significant bit at the 10-bit level, which is 0.1% of the full scale voltage.
2. Relative accuracy is defined as the deviation of the actual code transition points from a straight line drawn between the first code transition point and the final code transition point.
3. Resolution for which the device is guaranteed to have no missing codes.
4. Deviation of the reference voltage output over the operating temperature range from its 25°C value.
5. Maximum change in the final code transition point. This will also result in a linear change in all lower order codes.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$, $V_{EE} = -5V$, $T_A = 25°C$, $F_{CLK} = 5MHz$

	PARAMETER	TO	FROM	EDGE		MIN	TYP	MAX	UNITS
F_{CLK}	Max clock frequency					3.0[1]	4.0		MHz
t_{WCP}	Pos clk pulse width					90			nS
t_{WCN}	Neg clk pulse width					90			nS
t_{CONV}	Conversion time						$7.5/F_{CLK}$[2]		nS
t_W	START pulse width					100			nS
t_S	Set-up time	CLK	$\overline{START}$	HI-LOW		tbd	tbd		nS
$t_{P\ (DATA)}$	Access time	DB0-DB9	$\overline{OE}$	HI-LOW			tbd	tbd	nS
$t_{P\ (3\text{-}STATE)}$	Disable time	hi-Z	$\overline{OE}$	LOW-HI			tbd	tbd	nS
$t_{P\ (EDC)}$	Propagation delay	$\overline{EOC}$ hi	$\overline{OE}$	HI-LOW			tbd	tbd	nS

NOTES:
1. Maximum clock frequency. Subject to change before product release.
2. Frequency in MHz.

TIMING DIAGRAM



* Timing diagram shows internal logic operation for the sake of short cycle operation. Data outputs are in Hi-2 state until $\overline{OE}$ and $\overline{CS}$ are both brought to a logic low.

10-Bit High Speed Microprocessor-Compatible Analog to Digital Converter

SE/NE5030

CIRCUIT DESCRIPTION

The SE/NE5030 is a microprocessor compatible, high speed, 10-bit Analog-to-Digital converter. The device uses a new multi-step parallel conversion scheme[1] which determines two bits of the digital word in each conversion step, permitting a fast 2.5 microsecond conversion time.

Refer to the block diagram. The fullscale current of the DAC is V_{REF}/R. When conversion is initiated, the successive approximation register (SAR) directs the two MSB currents of the DAC (I9 and I8) to $\overline{Io}$ and the remaining bit currents of the DAC (including the DAC R/2R termination current) to Io1. This divides the input signal range into four equal subranges. The three latched comparators determine into which of these subranges the input voltage falls. The decoded outputs of these comparators determine the two MSBs (D9 and D8), which are stored in the SAR.

In each subsequent step, the SAR controls the DAC such that the complement of the previously determined bits are directed through Io2; the bits currently being determined are directed through $\overline{Io}$, and the remainder of the bits are directed through Io1. In this manner the subrange containing the analog input voltage in the previous step is divided into four smaller subranges and two bits of the digital output are determined. At the end of five steps the SAR contains a 10-bit binary code which accurately represents the input signal to within ±1/2 LSB.

FUNCTIONAL DESCRIPTION

With an external clock signal connected to the CLOCK IN pin, $\overline{CS}$ at a logic low, and $\overline{OE}$ at a logic high, a conversion cycle is initiated with the application of an external start pulse applied to the $\overline{START}$ pin. The SAR sequences through the conversion as described above. At the end of the conversion, the end-of-conversion flag ($\overline{EOC}$) goes low. The $\overline{EOC}$ flag can be used to interrupt a microprocessor or otherwise notify a processor or controller that a conversion is completed. $\overline{OE}$ may then be forced low (while holding $\overline{CS}$ low), enabling the three-state output buffers so that the converted word may be read. Bringing the $\overline{OE}$ pin low while the $\overline{CS}$ pin is low also resets the $\overline{EOC}$ flag to a logic high. It is recommended that $\overline{OE}$ be brought to a logic high prior to the application of another $\overline{START}$ pulse. If $\overline{OE}$ were to remain low during a conversion, the output buffers would be enabled and would switch states during the conversion. This switching can couple into the analog input through parasitic capacitances, causing erroneous conversion results.

The application of another START pulse while a conversion is in progress will halt the conversion in progress and begin a new conversion cycle. If a $\overline{START}$ pulse is received while the $\overline{CS}$ input is at a logic high, that $\overline{START}$ pulse is ignored. The outputs will be in the high impedance state as long as either $\overline{CS}$ or the $\overline{OE}$ input is at a logic high.

LOGIC INPUTS AND OUTPUTS

All the logic inputs ($\overline{BIPOLAR}$, CLOCK IN, $\overline{START}$, $\overline{CS}$, $\overline{OE}$) respond to TTL level signals and present one LS TTL load to the driving source. The logic outputs are capable of driving two TTL loads. If long digital lines or a heavily loaded bus must be driven, external logic buffers are recommended.

VOLTAGE REFERENCE

The internal voltage reference (2.5V ±0.2%) is of a second order-corrected design. The output voltage is trimmed at the wafer level by the "Zener zap" technique to have a temperature coefficient of less than ±10 ppm/°C (average) over the operating temperature range. $V_{REF\ OUT}$ (pin 1) and $V_{REF\ OUT}$ (pin 2) are not internally connected and should be connected together close to the device. The voltage reference output (pin 1) can provide up to 2mA to an external load for other system applications. The current drawn by any external load *must remain constant* during a conversion.

ANALOG INPUT

The analog input voltage to ge digitized is connected between V_{IN} (pin 5) and Analog Common (pin 6). The device operates in either a unipolar mode (input range of 0 to V_{REF}) or in a bipolar mode (input range of $-V_{REF}/2$ to $+V_{REF}/2$). The TTL compatible $\overline{BIPOLAR}$ input is used to select the mode.

When the $\overline{BIPOLAR}$ input is high, the device operates in the unipolar mode. The input range is then 0 to $+V_{REF}$ (2.5V nominal). The nominal value of the LSB is 2.44mV. The SE/NE5030 is designed to have a 1/2 LSB offset so that the analog input exactly corresponding to a given code will fall in the center of that code's input range. Thus, the ideal input voltage to cause the first transition (from 00 0000 0000 to 00 0000 0001) will occur for an input voltage of 1.22mV, and the final transition (from 11 1111 1110 to 11 1111 1111) will ideally occur for an input voltage of 2496.34mV, or 1.5 LSB below the 2.5V reference.

For bipolar operation, the $\overline{BIPOLAR}$ input is set to a logic low. This shifts the transfer curve of the A/D by $V_{REF}/2$ so that the input voltage range is now $-(V_{REF}/2)$ to $+(V_{REF}/2)$, or (−1.25V to +1.25V nominal). The ideal transition of code from 00 0000 0000 to 00 0000 0001 occurs at an input of −1248.78mV, and the final code transition (11 1111 1110 to 11 1111 1111 occurs at 1246.34mV.

The high input impedance of the SE/NE5030 analog input simplifies the requirements of the signal source driving the SE/NE5030, eliminating the need for specialized drive circuitry.

POWER SUPPLY DECOUPLING AND LAYOUT CONSIDERATIONS

Since one LSB of the SE/NE5030 input is just 2.44mV, good layout and grounding techniques are crucial to attaining optimum performance.

The power supplies should be filtered, well regulated, and free of high frequency noise. Use of noisy supplies will cause unstable output codes to be generated. The power supplies should be bypassed to Analog Common with tantalum or electrolytic capacitors in parallel with a small, high frequency bypass. Suitable bypasses would be 22μF electrolytic capacitors with 0.1μF ceramic capacitors in parallel with them. These capacitors should be located close to the device.

Analog Common and Digital Common are not connected internally and should be connected together as close to the device as possible. Low impedance analog and digital common returns are important for optimum performance. The power supply returns should be connected to the Digital Common of the device. The Analog Common is the ground reference point for the internal voltage and should be connected directly to the Analog Common reference point of the system.

Coupling between the digital lines and the Analog Input should be minimized by careful printed circuit board layout. The layout should attempt to locate the analog circuitry and their interconnections as far from the logic circuitry as is possible. Use of wire wrap techniques or plug-in type boards is not recommended.

NOTE:

1. M. Kolluri: "A Multi-Step Parallel 10-Bit 1.5μSec ADC," *ISSCC Digest of Technical Papers* , p 60−61; Feb 1984.

12-Bit D/A Converter

DAC800

DESCRIPTION

The DAC800 is a single-chip converter with 12-bit linearity, obtained without trimming. It is pin compatible with the industry standard DAC80 (no external reference can be used) and has a faster settling time. This converter has thin film application resistors, a low temperature coefficient bandgap reference, and an output amplifier (V models).

The DAC800 provides for both bipolar and unipolar outputs. The V models allow output ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. The current models have an output range of either ±1mA or 0 to −2mA.

The DAC800 has a maximum nonlinearity error of ±½ LSB over the full temperature range, 0°C to 70°C. Additionally, the DAC800 offers maximum total error over the full temperature range of ±0.15% of full-scale for unipolar operation and ±0.12% of full-scale for bipolar operation. The total error includes the effects of gain, offset, and linearity drift with gain and offset errors adjusted to zero at 25°C.

FEATURES

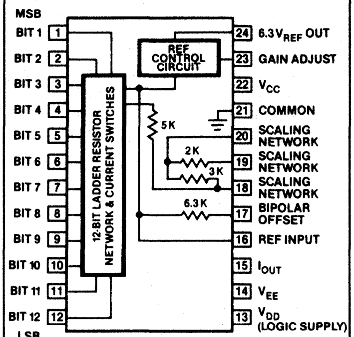
- **Maximum Nonlinearity ±½ LSB**
- **Guaranteed Monotonicity 0°C to 70°C**
- **Current or Voltage Output Models**
- **Internal Reference**
- **Unipolar and Bipolar Operation**
- **Compatible with TTL/LSTTL/CMOS**
- **No Laser Trimming**
- **Excellent Power Supply Rejection**

APPLICATIONS

- **Data Acquisition and Control Systems**
- **Analog-to-Digital Converter Systems**
- **Automatic Test Equipment**
- **Robotics**
- **Waveform Generation**

PIN CONFIGURATIONS

Current Model
F Package

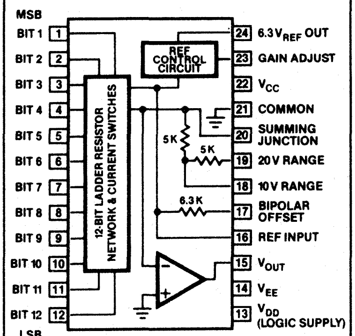


TOP VIEW

Order Number

DAC800IF

Voltage Model
F Package



TOP VIEW

Order Number

DAC800VF

4

AC ELECTRICAL CHARACTERISTICS $V_{CC}=15V$, $V_{EE}=-15V$, $V_{DD}=5V$, $0°C < T_A < 70°C$ (Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IH}	Logic Input High		2		16.5	V
V_{IL}	Logic Input Low		0		0.8	V
I_{IH}	Logic High Input Current	$V_{IN}=2.4V$			20	μA
I_{IL}	Logic Low Input Current	$V_{IN}=0.4V$	−20			μA
	Power Supply Sensitivity V_{CC}, V_{EE}, V_{DD}			±0.0005	±0.001	% of FSR/%V
	V_{CC}, V_{EE}		±13.5	±15	±16.5	V
	V_{DD} 5		4.5	5	16.5	V
	I_{CC}			11	14	mA
	I_{EE}		−20.	−17		mA
	I_{DD}			6.5	8	mA

NOTES:
1. Adjustable to zero with external trim potentiometer.
2. To maintain drift specs internal resistors must be used on current output model.
3. FSR means full-scale range and is 20V for ±10V range, 10V for ±5V range, etc.
4. Includes the effects of gain, offset, and linearity drift. Gain and offset errors are adjusted to zero at 25°C.
5. Power dissipation is an additional 20mW when V_{DD} is operated at +15V.
6. $R_L=2K$, $C_L=200pF$, $T_A=25°C$ for V models only.
7. $C_L=10pF$, $T_A=25°C$ for I models.
8. Typical operating conditions for Amplifier Duration Output Short Circuit to Ground is indefinite at this time.

12-Bit D / A Converter

DAC800

POWER SUPPLY CONNECTIONS

Any noise present on the power supply pins of the DAC800 creates additional error. For optimum performance this noise should be limited as much as possible. This can be accomplished by bypassing the power supply pins with appropriate capacitors. Decoupling capacitors on the order of 1μF are recommended with the best types being tantalum or electrolytic. Electrolytic capacitors have poor high frequency characteristics and, if used, should be paralleled with a 0.01μF ceramic capacitor.

LOGIC INPUTS

The logic inputs of the DAC800 are compatible with TTL, LSTTL, and CMOS over the operating range of V_{DD} (5V to 15V) as well as over temperature (0°C to 70°C). The input switching threshold is TTL (about 1.4V) and is independent of the supply voltage, V_{DD}.

Logic input coding for the DAC800 is complementary. The specific code will be complementary straight binary (CSB) for unipolar output connections and complementary offset binary (COB) for bipolar output connections. For bipolar output connections, complementary two's complement (CTC) can be realized by inverting the MSB with an external inverter. The relationship between the digital input and analog output for the three codes is shown in Table 1.

VOLTAGE REFERENCE

The DAC800 has an internal 6.3V reference with a ±1% tolerance. The reference is connected internally to the converter and to the bipolar offset resistor and to pin 16 which does not allow the use of an external reference. The reference is brought out on pin 24 for external use, if needed, and can typically supply 2.5mA. If the external load varies, an external buffer is recommended in order to isolate the reference from load variations.

EXTERNAL GAIN / OFFSET ADJUSTMENTS

The gain and offset of the DAC800 can be adjusted with external potentiometers. The potentiometer configuration required for gain adjustment is shown in Figure 1. The 10MΩ resistor should have a tolerance of 20% or less and the potentiometer and 10MΩ resistor should have a temperature coefficient of 200ppm / °C or less.

The potentiometer configuration required for offset adjustment is shown in Figure 2 and its equivalent circuit in Figure 3. From the equivalent circuit it can be seen that this configuration adds/subtracts a current from the converter output current. The 3.9MΩ resistor should have a tolerance of 20% or less and the potentiometer and 3.8MΩ resistor should have a temperature coefficient of 200 ppm/ °C or less. Both adjustment circuits should be located close to the DAC800 to prevent noise pickup. If full-scale accuracy is not required, then the gain adjust pin may be grounded to minimize noise pick-up.

The effects of gain and offset adjustment are shown in Figures 4 and 5. Figure 4 shows that gain adjustment rotates the transfer function about the origin and has no impact on the origin. Figure 5 shows that offset adjustment translates the transfer function along the ANALOG OUTPUT axis. Note that this changes the output for full-scale. The objective of the adjustment procedure is to fix the end points of the transfer function at the ideal points. For this reason the adjustment sequence must be to first adjust the offset and then the gain. Offset adjustment is accomplished by setting all logic inputs to a logic high ("1") and adjusting the offset so that the output corresponds to its most negative value (zero for unipolar outputs and −full-scale for bipolar outputs). Gain adjustment is accomplished by setting all logic inputs to a logic low ("0") and adjusting the gain such that the output corresponds to its most positive value (full-scale −1 LSB).

VOLTAGE MODEL OUTPUT CONNECTIONS

The DAC800 voltage models have internal scaling resistors which provide output ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. The use of the internal resistors minimizes gain and offset drift since excellent thermal tracking with other on-chip components limits this effect. Figures 6a, b and c show the different output configurations.

Table 1. Coding Relationships

DIGITAL INPUT	ANALOG OUTPUT		
	CSB	COB	CTC
MSB LSB			
000000000000	+Full-Scale −1 LSB	+Full-Scale −1 LSB	−1 LSB
011111111111	+½ Full-Scale	Zero	− Full-Scale
100000000000	+½ Full-Scale −1 LSB	−1 LSB	+Full-Scale −1 LSB
111111111111	Zero	− Full-Scale	Zero

12-Bit D/A Converter — DAC800

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Temperature Range		
Operating	0 to 70	°C
Storage	−65 to +150	°C
Power Supply		
V_{CC}, V_{EE}	±16.5	V
V_{DD}	+16.5	V
Logic Levels		
High	+16.5	V
Low	0	V

NOTE:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 15V$, $V_{EE} = -15V$, $V_{DD} = 5V$, $0°C < T_A < 70°C$ (Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		12			Bits
	Monotonicity		12			Bits
NL	Nonlinearity				±1/2	LSB
DNL	Differential Nonlinearity			±1/2	±1	LSB
	Gain Error[1]	$T_A = 25°C$		±0.1	±0.2	% of FSR
	Gain Tempco			±10	±30	ppm/°C
	Offset Error[1]			±0.05	±0.15	% of FSR[3]
	Offset Tempco[2]	Unipolar Connection		±1	±3	ppm of FSR/°C
	Offset Tempco[2]	Bipolar Connection		±7	±15	ppm of FSR/°C
	Bipolar Drift	Full-Scale Drift for Bipolar Connection		±10	±25	ppm of FSR/°C
	Total Error[4]	Unipolar Connection		±0.06	±0.15	% of FSR
	Total Error[4]	Bipolar Connection		±0.05	±0.12	% of FSR
t_S	Settling Time to 0.01% of FSR[6]	20V Range		3	5	μs
t_S	Settling Time to 0.01% of FSR[6]	10V Range		2.5	4	μs
t_S	Settling Time to 0.01% of FSR[6]	1 LSB Change, Major Carry		1.5		μs
t_S	Settling Time to 0.01% of FSR[7]	10 to 100Ω Load		300		ns
t_S	Settling Time to 0.01% of FSR[7]	1kΩ Load		1		μs
	Full-Scale Current	I Model Only	1.7	2	2.3	mA
	Converter Output Impedance	I Model Only		10		MΩ
	Converter Output Compliance	I Model Only	−2.5		+2.5	V
	Amplifier Slew Rate[6]		10	15		V/μs
	Amplifier Output Current	V Model Only	±5			mA
	Amplifier DC Output Impedance	V Model Only		0.05		Ω
	Amplifier Duration Output Short Circuit to Ground[8]	V Model Only				
V_{REF}	Reference Voltage Output		6.23	6.30	6.37	V
	Reference Voltage Tempco			±10	±30	ppm/°C
	Reference Output Source Current		1.5	2.5		mA

12-Bit D/A Converter DAC800

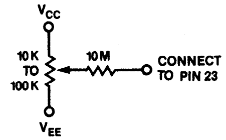


Figure 1. Gain Adjust Circuit

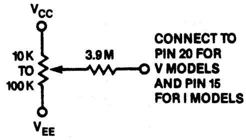


Figure 2. Offset Adjust Circuit

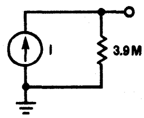


Figure 3. Offset Adjust Equivalent Circuit

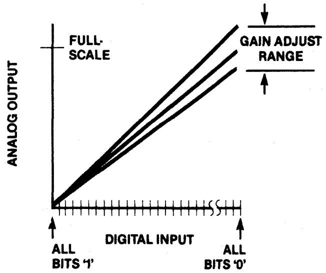


Figure 4. Gain Adjust Effects

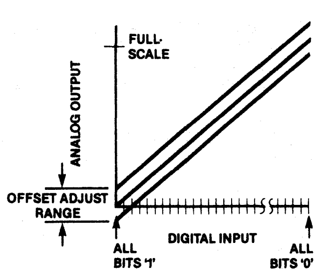
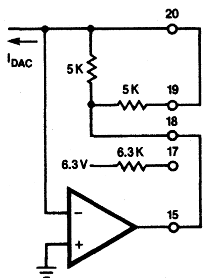
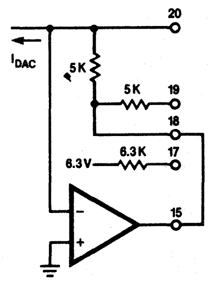


Figure 5. Offset Adjust Effects



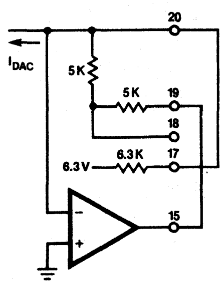
*Connect pin 17 to pin 20 for ±2.5V Range and to ground for 0 to 5V Range

a. Connections for 0 to 5V Range and ±2.5V Range (V model)



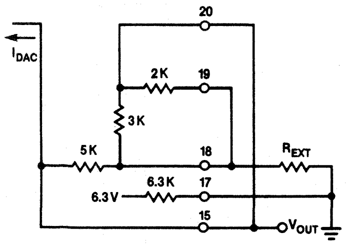
*Connect pin 17 to pin 20 for ±5V Range and to ground for 0 to 10V Range

b. Connections for 0 to 10V Range and ±5V Range (V model)

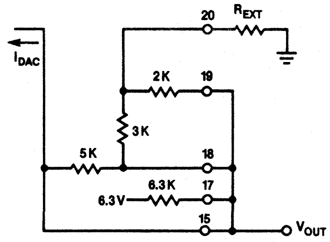


c. Connections for ±10V Range (V model)

Figure 6.



a. Connections for 0 to −2V Range (I model)



b. Connections for +1V Range (I model)

Figure 7.

CURRENT MODEL OUTPUT CONNECTIONS

Internal resistors are provided for the current models which can be used with an external op amp or configured as a resistive load for output ranges of 0 to −2V or ±1V. Use of these internal resistors is required to maintain gain and bipolar offset drift specifications.

Output ranges of 0 to −2V and ±1V are obtainable with the addition of a single external resistor (excluding the gain and offset adjustment components). Figures 7a and b show the necessary connections for these output ranges. The internal resistors of the DAC800 have wide tolerances and the external resistor, R_{ext} will have to be selected for each unit. Nominal values will be 32Ω for the unipolar connection and 0Ω for the bipolar connection.

The current output can also be used to drive the summing junction of an external op amp used as a voltage to current converter. This has the advantage of faster settling time than the voltage model. Figure 8 shows the general configuration and Table 2 lists the available output ranges and required connections.

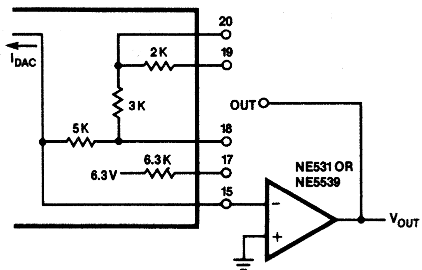


Figure 8. General Configuration for Current Model Using External Op Amp

Table 2. Current Model Connection for Various Output Ranges

OUTPUT RANGE	CONNECT		
	OUT TO	19 TO	17 TO
±10V	19	Out	15
±5V	18	NC	15
±2.5V	18	15	15
0 to +10V	18	NC	GND
0 to +5V	18	15	GND

8-Bit Microprocessor-Compatible D/A Converter

SE/NE5018

DESCRIPTION

The NE5018 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

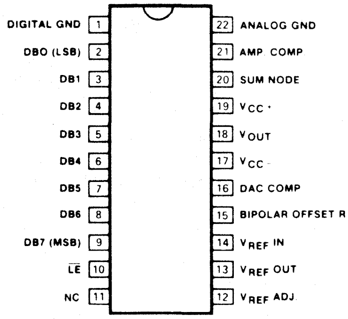
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/2 LSB (.19%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other μP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

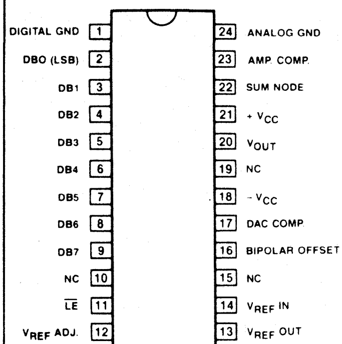
PIN CONFIGURATION

F,N PACKAGE



ORDER NUMBERS
SE/NE5018F,N

D² PACKAGE



TOP VIEW
ORDER NUMBER
NE5018D²

NOTES:
1. SOL-Released in Large SO package only
2. SOL and non-standard pinout
3. SO and non-standard pinouts

BLOCK DIAGRAM

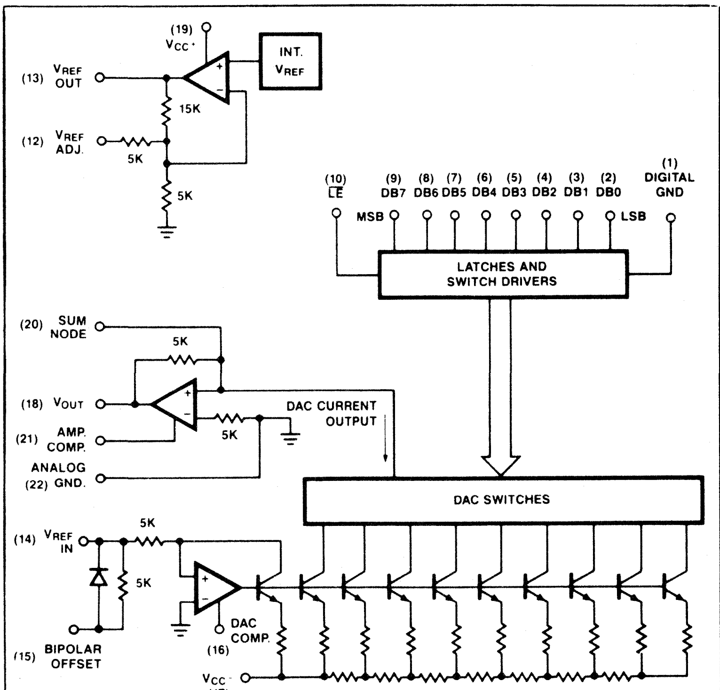


Figure 1

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5018	−55 to +125	°C
	NE5018	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018, $-55°C \leq T_A \leq 125°C$, NE5018, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

	PARAMETER	TEST CONDITIONS	SE5018 Min	SE5018 Typ	SE5018 Max	NE5018 Min	NE5018 Typ	NE5018 Max	UNIT
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.19	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	9.50	9.961	10.50	9.50	9.961	10.50	V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	4.5	+4.961	5.5	4.5	+4.961	5.5	V
			-5.04	−5.000	-4.960	5.04	−5.000	4.960	
V_{ZS}	Zero scale voltage		-30	5	+30	-30	5	+30	mV
I_{OS}	Output short circuit current	$T_A = 25°C$, $V_{OUT} = 0V$		15	40		15	40	mA
PSR+(out)	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
PSR−(out)	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

4

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018, $-55°C \leq T_A \leq 125°C$, NE5018, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE/5018			NE5018			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 8			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$, $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01		.003	.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$, $T_A = 25°C$		60			60		ppm/°C
Z_{IN}	DAC V_{REF} IN input impedance	$I_{REF} = 1.0mA$ $T_A = 25°C$	4.15	5.0	5.85	4.15	5.0	5.85	KΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE
1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[2] $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5018			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	±½ LSB	Input	All bits low to high[3]		1.8		μs
T_{SHL}	Settling time	±½ LSB	Input	All bits high to low[4]		2.3		μs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[3]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[4]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[3,4]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[5]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[6]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	2, 7	100			ns
t_h	Hold time	Input	$\overline{LE}$	2, 7	50			ns
t_{pw}	Latch enable pulse width			2, 7	150			ns

NOTES
2. Refer to Figure 3.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. See Figure 10.
8. For reference currents > 3mA, use of an external buffer is required.

8-Bit Microprocessor-Compatible D/A Converter SE/NE5018

DC PARAMETRIC TEST CONFIGURATION

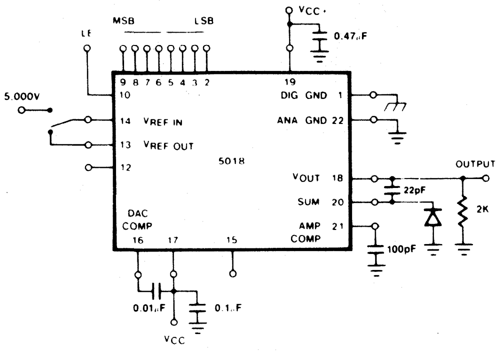


Figure 2

AC PARAMETRIC TEST CONFIGUTATION

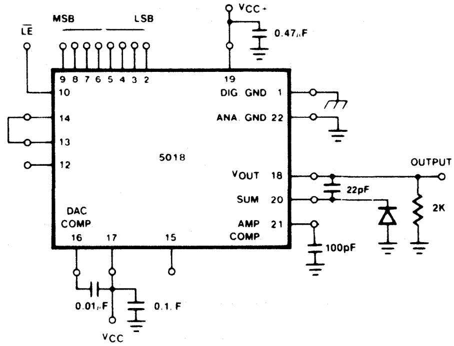


Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0-10V)

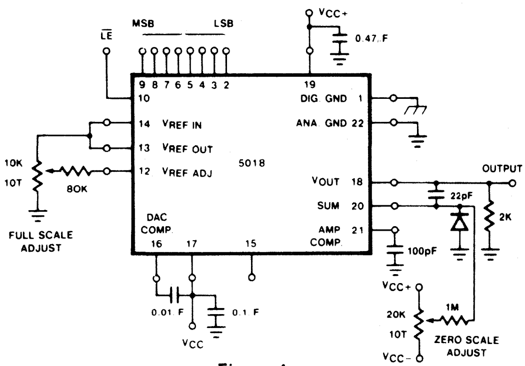


Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

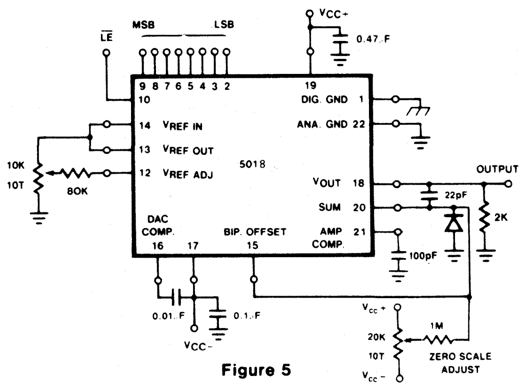


Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

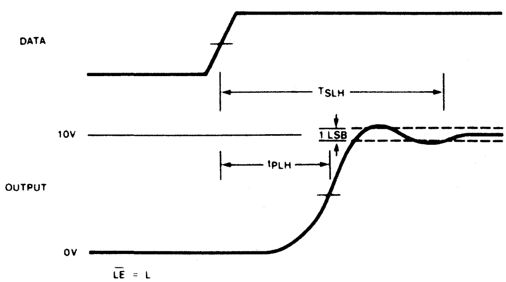


Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

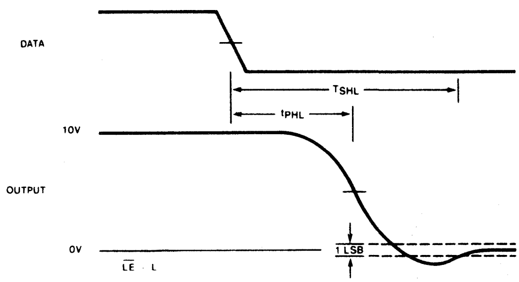


Figure 7

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

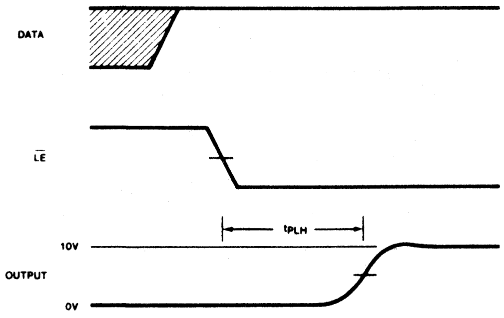


Figure 8

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

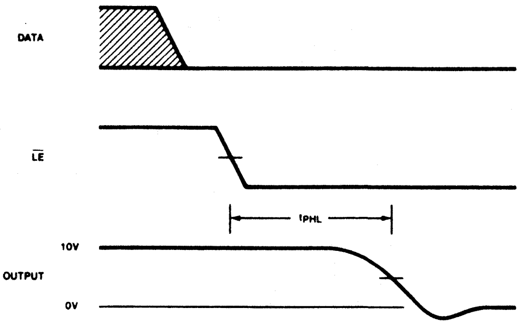


Figure 9

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

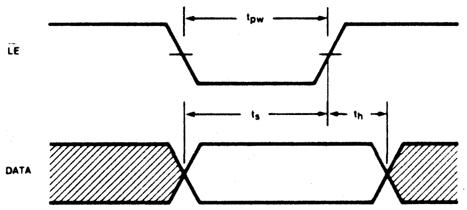


Figure 10

8-Bit Microprocessor-Compatible D/A Converter

SE/NE5019

DESCRIPTION

The NE5019 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

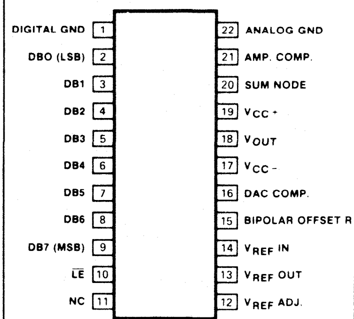
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/4 LSB (.1%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other µP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

PIN CONFIGURATION

F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE5019F SE5019F
NE5019N

4

BLOCK DIAGRAM

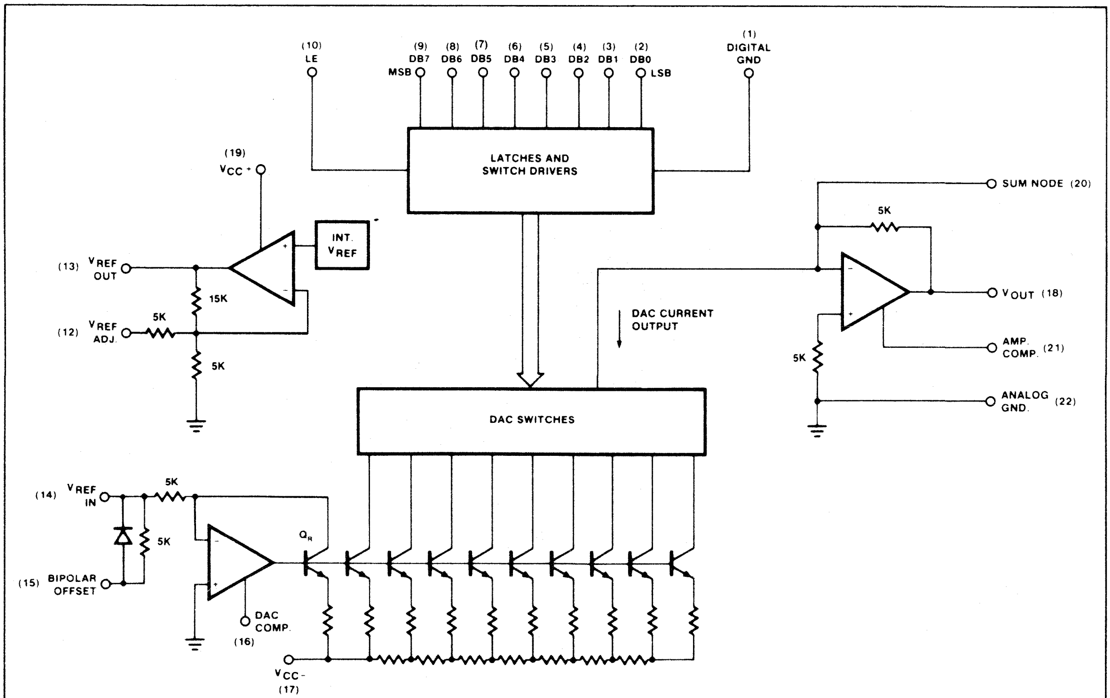


Figure 1

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5019	−55 to +125	°C
	NE5019	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019, $-55°C \leq T_A \leq 125°C$, NE5019, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

	PARAMETER	TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\,IN} = 5.000V$, $T_A = 25°C$	9.50	9.961	10.50	9.50	9.961	10.50	V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\,IN} = 5.000V$, $T_A = 25°C$	4.5 -5.040	+4.961 −5.000	5.5 -4.960	4.5 -5.040	+4.961 −5.000	5.5 -4.960	V
V_{ZS}	Zero scale voltage		-30	5	+30	-30	5	+30	mV
I_{OS}	Output short circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		15	40		15	40	mA
PSR+(out)	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\,IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
PSR−(out)	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\,IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\,IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

NOTE
1. Refer to Figure 2

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leq T_A \leq 125°C$, NE5019. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 8			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$, $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
$PSR-_{REF}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01		.003	.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$, $T_A = 25°C$		60			60		ppm/°C
Z_{IN}	DAC $V_{REF}IN$ input impedance	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.15	5.0	5.85	4.15	5.0	5.85	KΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE

1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[2] $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5019			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits low to high[3]		1.8		μs
T_{SHL}	Settling time	± ½ LSB	Input	All bits high to low[4]		2.3		μs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[3]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[4]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[3,4]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[5]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[6]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	2, 7	100			ns
t_h	Hold time	Input	$\overline{LE}$	2, 7	50			ns
t_{pw}	Latch enable pulse width			2, 7	150			ns

NOTES

2. Refer to Figure 3.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. See Figure 10.
8. For reference currents > 3mA, use of an external buffer is required.

8-Bit Microprocessor-Compatible D/A Converter — SE/NE5019

DC PARAMETRIC TEST CONFIGURATION

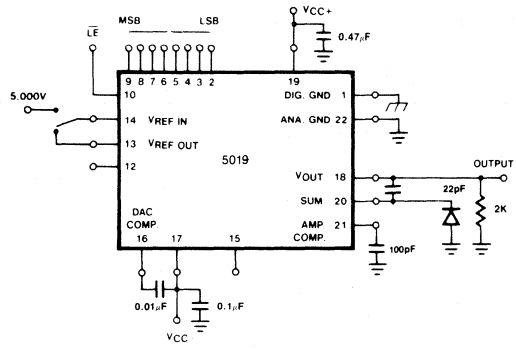


Figure 2

AC PARAMETRIC TEST CONF'GUTATION

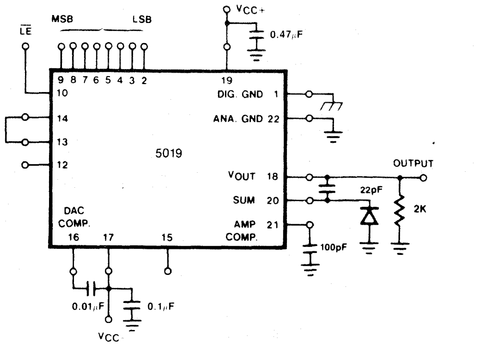


Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0-10V)

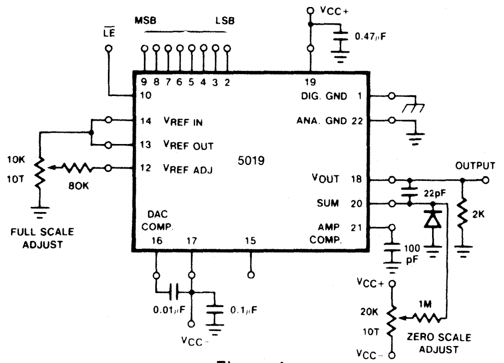


Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

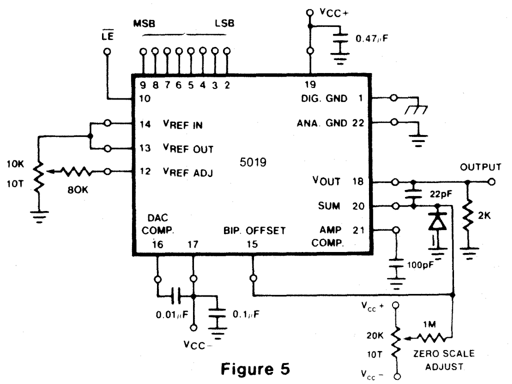


Figure 5

SETTLING TIME AND PROPAGATON DELAY, LOW TO HIGH DATA

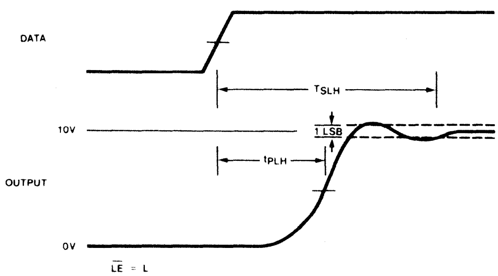


Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

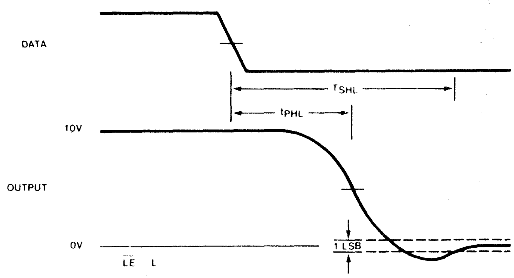


Figure 7

8-Bit Microprocessor-Compatible D/A Converter

SE/NE5019

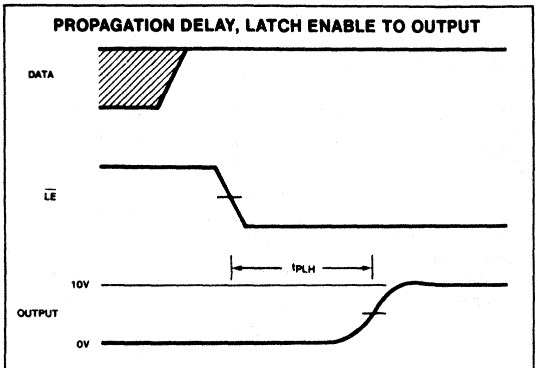


Figure 8

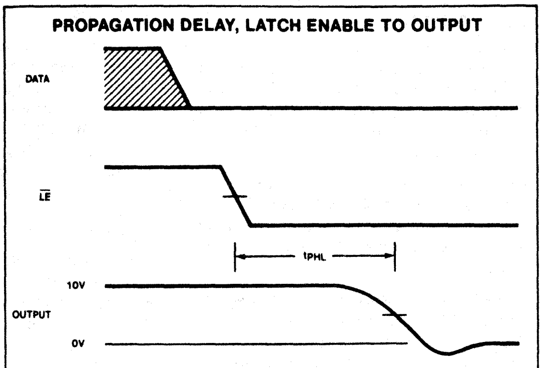


Figure 9

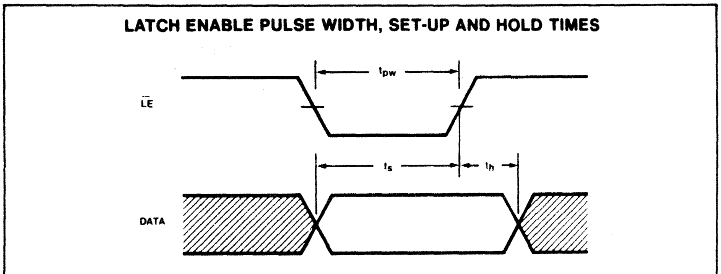


Figure 10

10-Bit Microprocessor-Compatible D/A Converter

SE/NE5020

DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital to analog converter subsystem. This device offers 10-bit resolution and ±0.1% accuracy and monotonicity guaranteed over full operating temperature range.

Low loading latches, adjustable logic thresholds and addressing capability allow the NE5020 to directly interface with most microprocessor and logic controlled systems.

The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

FEATURES

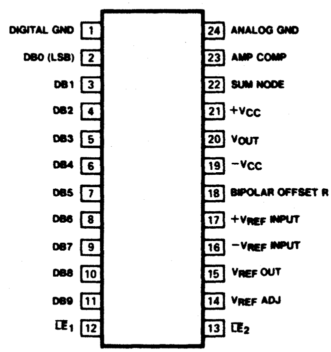
- **10-bit resolution**
- **Guaranteed monotonicity over operating range**
- **±0.1% relative accuracy**
- **Unipolar (0V to +10V) and Bipolar (±5V) output range**
- **Logic bus compatible**
- **5μsec settling time**

APPLICATIONS

- **Precision 10-bit D/A converters**
- **10-bit Analog to Digital converters**
- **Programmable power supplies**
- **Test equipment**
- **Measurement instruments**

PIN CONFIGURATION

F, N PACKAGE



ORDER NUMBERS
NE5020F
NE5020N

BLOCK DIAGRAM

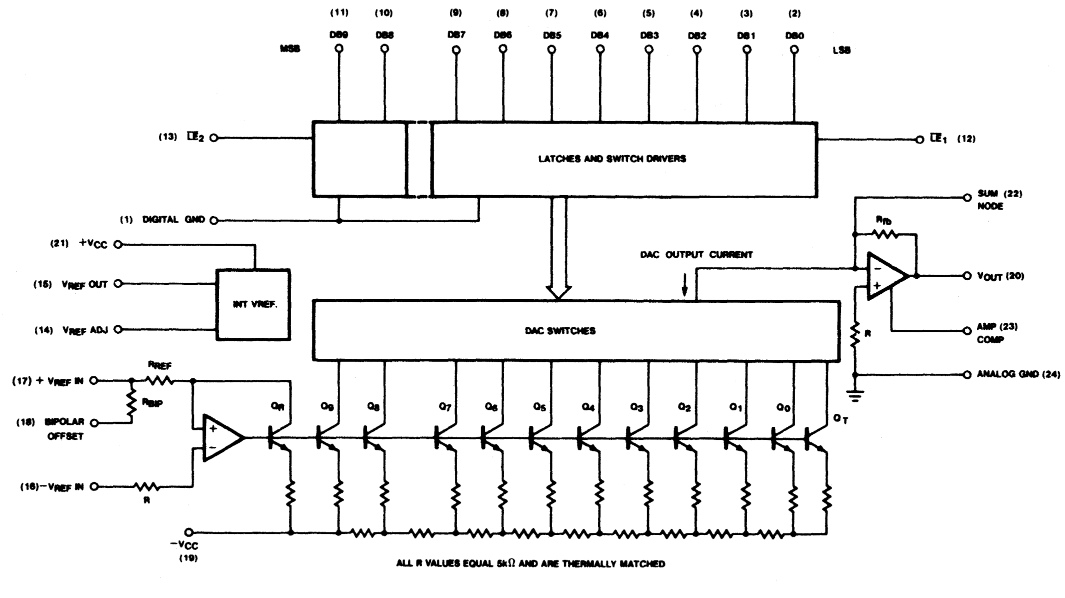


Figure 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
V_{REF} IN	Voltage at $+V_{REF}$ input	12	V
V_{REF} ADJ	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	F package	1000	mW
T_A	Operating temperature range		
	NE5020	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	NE5020			UNIT
			Min	Typ	Max	
	Resolution				10	Bits
	Monotonicity				10	Bits
	Relative accuracy				±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15	16.5	V
$V_{CC}-$	Negative supply voltage		−11.4	−15	−16.5	V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V<V_{IN}<18V$		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V<V_{IN}<0.8V$		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN}$ = 5.000V, T_A = 25°C	9.5	9.9902	10.5	V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\ IN}$ = 5.000V, T_A = 25°C	4.5 -5.040	4.9902 −5.000	5.5 -4.960	V
V_{ZS}	Zero scale voltage	Unipolar operation	-30	5	+30	mV
I_{OS}	Output short circuit current	T_A = 25°C V_{OUT} = 0V		±15	±40	mA
PSR+(out)	Output power supply rejection (+)	V− = −15V, 13.5V≤V+≤16.5V, external $V_{REF\ IN}$ = 5.000V		.001	.01	%FS/ %VS
PSR−(out)	Output power supply rejection (−)	V+ = 15V, −13.5V≤V−≤−16.5V, external $V_{REF\ IN}$ = 5.000V		.001	.01	%FS/ %VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN}$ = 5.000V		20		ppmFS /°C
TC_{ZS}	Zero scale temperature coefficient			5		ppmFS /°C

NOTE
1. Refer to Figure 2.

10-Bit Microprocessor-Compatible D/A Converter — SE/NE5020

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	NE5020			UNIT
			Min	Typ	Max	
I_{REF}[2]	Reference output current				3	mA
$I_{REF\ SC}$	Reference short circuit current	$T_A = 25°C$, $V_{REF\ OUT} = 0V$		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01	%VR/%VS
$PSR-_{REF}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60		ppm/°C
Z_{IN}	DAC $V_{REF}IN$ input impedance	$I_{REF} = 1.0mA$		5.0		kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435	mW

NOTE
1. Refer to Figure 2.
2. For I_{REF} OUT greater than 3mA, an external buffer is required.

AC ELECTRICAL CHARACTERISTICS[3] $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	NE5020			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits low to high[4]		5		µs
T_{SHL}	Settling time	± ½ LSB	Input	All bits high to low[5]		5		µs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[4]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[5]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[4,5]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[6]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[7]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	3, 8	100			ns
t_h	Hold time	Input	$\overline{LE}$	3, 8	50			ns
t_{pw}	Latch enable pulse width			3, 8	150			ns

NOTES
3. Refer to Figure 3.
4. See Figure 6.
5. See Figure 7.
6. See Figure 8.
7. See Figure 9.
8. See Figure 10.

DC PARAMETRIC TEST CONFIGURATION

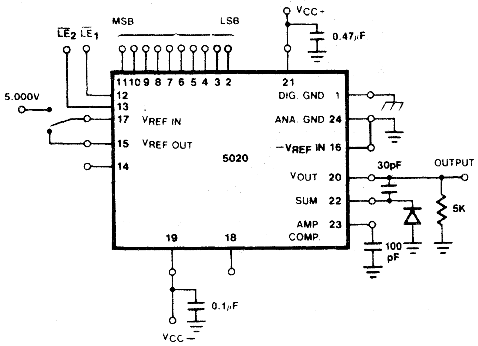


Figure 2

AC PARAMETRIC TEST CONFIGURATION

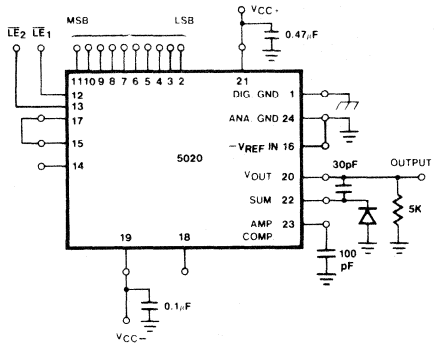


Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0–10V)

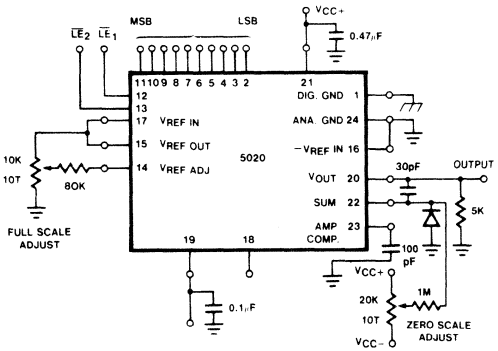


Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

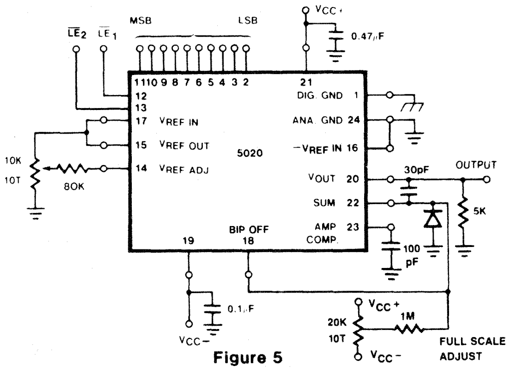


Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

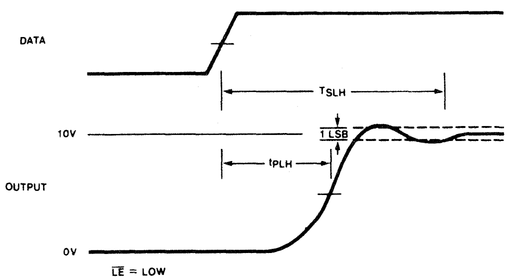


Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

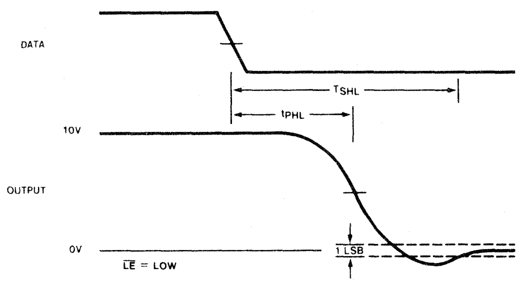


Figure 7

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

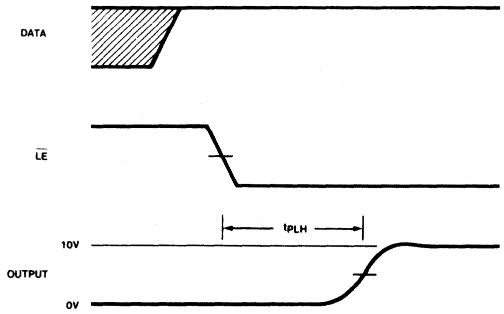


Figure 8

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

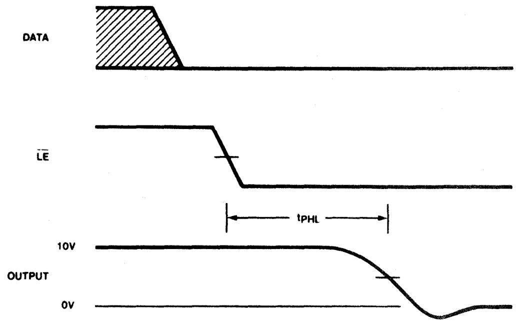


Figure 9

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

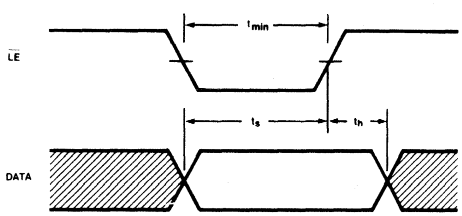


Figure 10

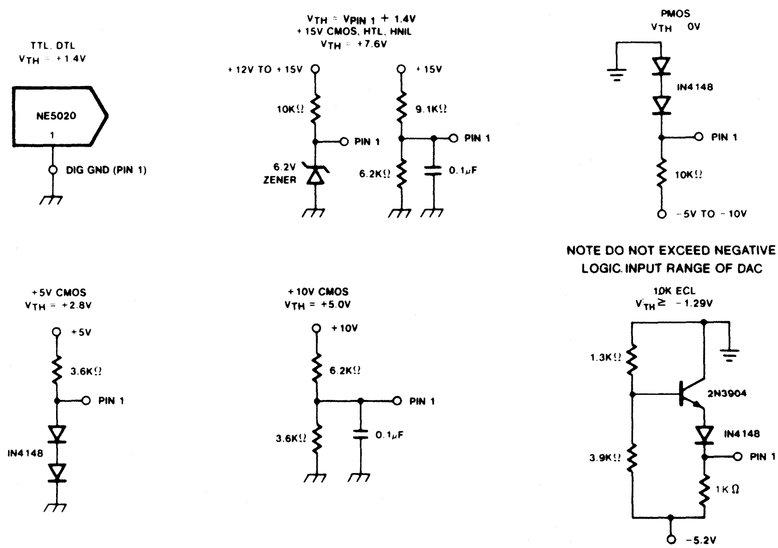


Figure 11

10-Bit Microprocessor-Compatible D/A Converter SE/NE5020

CIRCUIT DESCRIPTION

The NE5020 provides ten data latches, an internal voltage reference, application resistors, and a scaled output voltage, in addition to the basic DAC components (see block diagram, figure 1).

Latch Circuit

Digital interface with the NE5020 is readily accomplished through the use of two latch enable ports ($\overline{LE}_1$ and $\overline{LE}_2$) and ten data input latches. $\overline{LE}_2$ controls the two most significant bits of data (DB_9 and DB_8) while $\overline{LE}_1$ controls the eight lesser significant bits (DB_7 through DB_ϕ). Both the latch enable ports ($\overline{LE}$) and the data inputs are static and threshold sensitive. When the latch enable ports ($\overline{LE}$) are high (Logic '1') the data inputs become very high impedances and essentially disappear from the data bus. Addressing the $\overline{LE}$ with a low (Logic '0') the latches become active and adapt the logic states present on the data bus. During this state, the output of the DAC will change to the value proportional to the data bus value. When the latch enable returns to a high state, the selected set of data inputs (i.e., depending on which $\overline{LE}$ goes high) 'memorize' the data bus logic states and the output changes to the unique output value corresponding to the binary word in the latch.

The data inputs are inactive and high impedance (typically requiring $-2\mu A$ for low (.8V max) or $0.1\mu A$ for high (2.0V min)) when the $\overline{LE}$ is high. Any changes on the data bus with $\overline{LE}$ high will have no effect on the DAC output.

The digital logic inputs ($\overline{LE}$ and DB) for the NE5020 utilize a differential input logic system with a threshold level of +1.4 volts with respect to the voltage level on the digital ground pin (Pin 1). Figure 11 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

To be compatible with a bus orientated system the DAC should respond in as short a period as possible to insure full utilization of the microprocessor, controller and I/O control lines. Figure 10 shows the typical timing requirements of the latch and data lines. This figure indicates that data on the data bus should be stable for at least 50nsec after $\overline{LE}$ is changed to a high state.

The independent $\overline{LE}$ ($\overline{LE}_1$ and $\overline{LE}_2$) lines allow for direct interface from an 8 bit data bus (see figure 12). Data for the two MSB's is supplied and stored when $\overline{LE}_2$ is activated low and returned high according to the NE5020 timing requirements. Then $\overline{LE}_1$ is activated low and the remaining eight LSB's of data are transferred into the DAC. With $\overline{LE}_1$ returning high the loading of ten bit data word from an eight bit data bus is complete.

Occasionally the analog output must change to its data value within one data address operation. This is no problem using the NE5020 on a 16 bit bus or any other data bus with 10 or greater data bits.

This can be accomplished from an 8 bit data bus by utilizing an external latch circuit to preload the two MSB data values. Figure 13 shows the circuit configuration.

After preloading (via $\overline{LE}$ pre-load) the external latch with the two MSB values, $\overline{LE}_2$ is activated low and the eight LSB's and the

NE5020 µP INTERFACE 8-BIT DATA BUS EXAMPLE

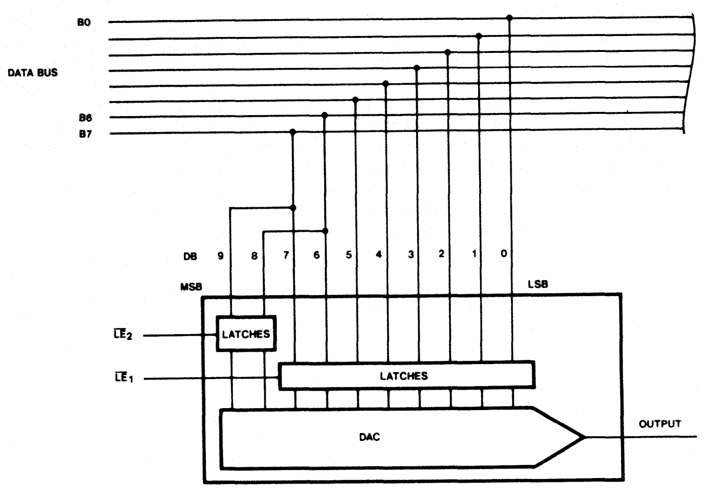


Figure 12

PRELOADING THE 2 MSB'S TO PROVIDE A SINGLE STEP OUTPUT

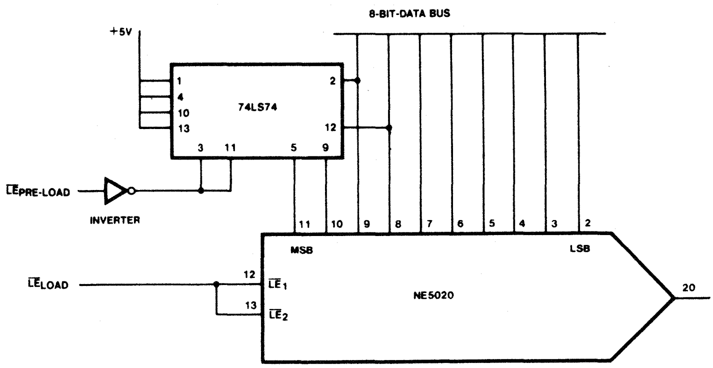


Figure 13

two MSB's are concurrently loaded into the DAC in one address operation. This permits the DAC output to make its appropriate change at one time.

Reference Interface

The NE5020 contains an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5 volt reference output. Providing a $V_{REF}ADJ$ (pin 14) allows trimming of the reference output. Utilization of the adjust circuit shown in figure 16 performs not only V_{REF} adjustment but also full scale output adjust. Notice that the $V_{REF}ADJ$ pin is essentially the sum node of an op amp and is sensitive to excessive node capacitance. Any capacitance on the node can be minimized by placing the external resistors as close as possible to the $V_{REF}ADJ$ pin and observing good layout practices.

The V_{REF} out node can drive loads greater than the DAC V_{REF} input requirements and can be used as an excellent system voltage reference. However, to minimize load effects on the DAC system accuracy, it is recommended that a buffer amplifier is used.

Input Amplifier

The DAC reference amplifier is a high gain internally compensated op amp used to convert the input reference voltage to a precision bias current for the DAC ladder network.

Figure 1 details the input reference amplifier and current ladder. The voltage to current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5 volt V_{REF}. This current sets the input bias to the ladder network. Data bit 9 (DB_9)(Q_9), when turned on, will mirror this current and will contribute 1mA to the output. DB_8 (Q_8) will contribute ½ of that value or 0.5mA and so on. These current values act as current sinks and will add at the sum node to produce a DAC ladder to sum node function of:

$$I_{OUT} = \frac{2V_{REF}}{R_{REF}}\left(\frac{DB9}{2} + \frac{DB8}{4} + \frac{DB7}{8} + \frac{DB6}{16} + \frac{DB5}{32} + \frac{DB4}{64} + \frac{DB3}{128} + \frac{DB2}{256} + \frac{DB1}{512} + \frac{DB0}{1024}\right).$$

Because of the fixed internal compensation of the reference amp, the slew rate is limited to typically 0.7V/μsec and source impedances at the V_{REF} INPUT greater than 5kΩ should be avoided to maintain stability.

The $-V_{REF\ INPUT}$ pin is uncommitted to allow utilization of negative polarity reference voltages. In this mode $+V_{REF\ INPUT}$ is grounded and the negative reference is tied directly to the $-V_{REF\ INPUT}$. The $-V_{REF\ INPUT}$ contains a 5kΩ resistor that matches a like resistor in the $+V_{REF\ INPUT}$ to reduce voltage offset caused by op amp input bias currents.

Output Amplifier and Interface

The NE5020 provides an on chip output op amp to eliminate the need for additional external active circuits. Its two stage design with feed forward compensation allows it to slew at 15V/μsec and settle to within ±½LSB in 5μsec. These times are typical when driving the rated loads of $R_L \geq 5k$ and $C_L \leq 50pF$ with recommended values of C_{FF} = 1nF and C_{FB} = 30pF. Typical input offset voltages of 5mV and 50k open loop gain insure an accurate current to voltage conversion is performed when using the on chip R_{FB} resistor. R_{FB} is matched to R_{REF} and R_{BIP} to maintain accurate voltage gain over operating conditions. The diode shown from ground to sum node prevents the DAC current switches from saturating the op amp during large signal transitions which would otherwise increase the settling time.

The output op amp also incorporates output short circuit protection for both positive and negative excursions. During this fault condition I_{OUT} will limit at ±15mA typical. Recovery from this condition to rated accuracy will be determined by duration of short circuit and die temperature stabilization.

Bipolar Output Voltage

The NE5020 includes a thermally matched resistor, R_{BIP}, to offset the output voltage by 5 volts to obtain −5V to +5V output voltage range operation. This is accomplished by shorting pins 18 and 22 (see figure 14). This connection produces a current equal to ($V_{REF\ IN} - V_{sum\ node}$) ÷ R_{BIP}, (1mA nominal), which is injected into the sum node. Since full scale current out is approximately 2mA (1.9980mA), (2mA − 1mA)5k = 5V will appear at the output. For zero DAC output currents, 1mA is still injected into sum mode and V_{OUT} = −(5k)(1mA) = −5V. Zero scale adjust and full scale adjust are performed as described below, noting that full scale voltage is now approximately +5 volts, zero scale adjust may be used to trim V_{OUT} = 0.00 with the MSB high or V_{OUT} = −5.0V with all bits off.

Zero Scale Adjustment

The method of trimming the small offset error that may exist when all data bits are low is shown in figure 15. The trim is the result of injecting a current from resistor R_2 that counteracts the error current. Adjusting potentiometer R_1 until V_{OUT} equals 0.000 volts in the unipolar mode or −5.000 volts in the bipolar mode (see bipolar section) accomplishes this trim.

Full Scale Adjustment

A recommended full scale adjustment circuit when using the internal voltage reference is shown in figure 16. Potentiometer R_3 is adjusted until V_{OUT} equals 9.99023V. In many applications where the absolute accu-

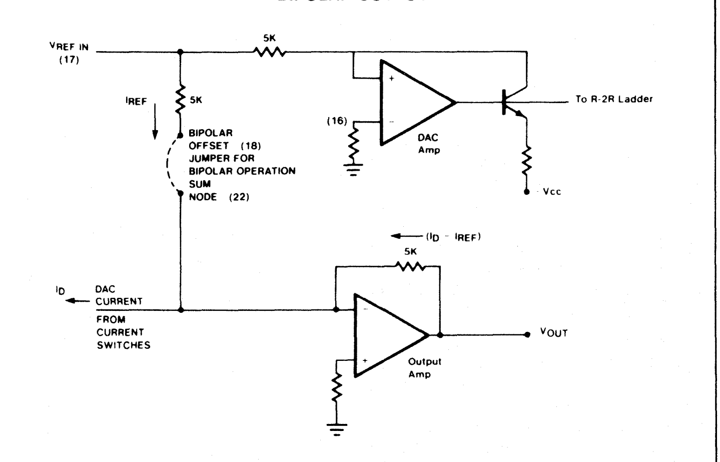


Figure 14

racy of full scale is of low importance when compared to the other system accuracy factors, then this adjustment circuit is optional.

As resistors R_{REF}, R_{fb} and R_{BIP} shown in figure 1 are integrated in close proximity, they match and track in value closely over wide ambient temperature variations. Typical matching is less than ±0.3% which implies that typical full scale (or gain) error is less than ±0.3% of ideal full scale value.

ZERO SCALE ADJUSTMENT

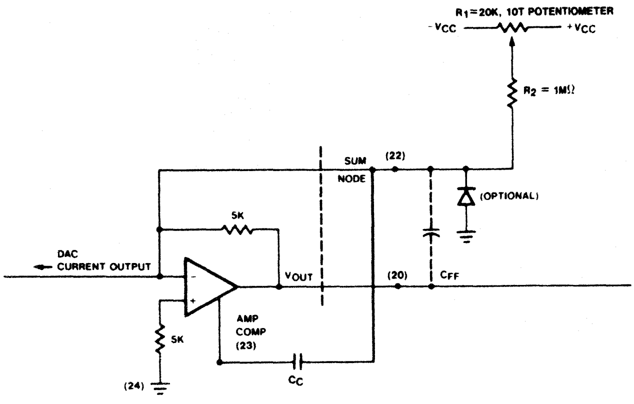


Figure 15

REFERENCE ADJUST CIRCUIT

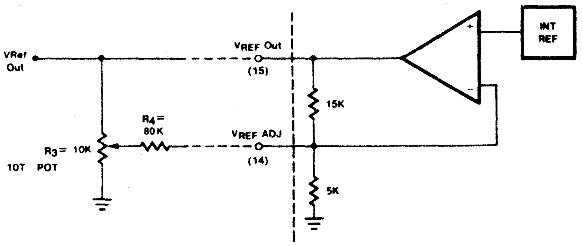


Figure 16

Triple 4-Bit RGB DAC

NE5150/NE5151

DESCRIPTION

The NE5150/5151 are triple 4-bit DAC's intended for use in graphic display systems. They are a high performance — yet cost effective — means of interfacing digital memory and a CRT. The NE5150 is a single integrated circuit chip containing special input buffers, an ECL static RAM, high-speed latches, and three 4-bit DAC's. The input buffers are *user* selectable as either ECL or TTL compatible. The RAM is organized as 16 x 12, so that 16 "color words" can be down loaded from the pixel memory into the chip memory. Each 12-bit word represents 4 bits of red, 4 bits of green and 4 bits of blue information. This system gives 4096 possible colors. The RAM is fast enough to completely reload during the *horizontal* retrace time. The latches resynchronize the digital data to the DAC's to prevent glitches. The DAC's include all the composite video functions to make the output waveforms meet RS170 and RS343 standards, and produce 1VPP into 75 ohms. The composite functions (reference white, bright, blank, and sync) are latched to prevent screen-edge distortions generally found on "video DAC's." External components are kept to an absolute minimum (bypass capacitors only as needed) by including all reference generation circuitry and termination resistors on chip, by building in high-frequency PSRR (eliminating separate V_{EE}'s and costly power supplies and filtering), and by using a single-ended clock. The guaranteed maximum operating frequency is 80MHz over the commercial temperature range. The device is housed in a standard 24-pin package and consumes less than 1W of power.

The NE5151 is a simplified version of the NE5150, including all functions except the memory. Maximum operating frequency is 150MHz.

FEATURES

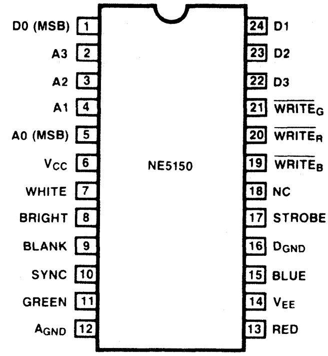
- **Single chip**
- **On-board ECL static RAM**
- **4096 colors**
- **ECL and TTL compatible**
- **80MHz update rate (NE5150)**
- **Low power and cost**
- **Drives 75-ohm cable directly**
- **Internal reference**
- **40dB PSRR**
- **No external components necessary**

APPLICATIONS

- **Bit-Map graphics**
- **Super high-speed DAC**
- **Home computers**
- **Raster-Scan displays**

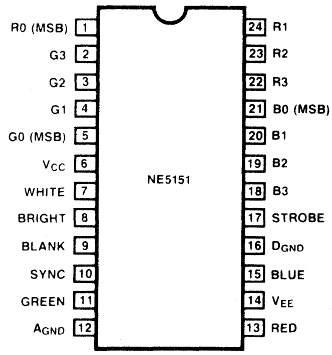
PIN CONFIGURATIONS

NE5150-F PACKAGE



TOP VIEW
Order Number
NE5150F

NE5151-F PACKAGE

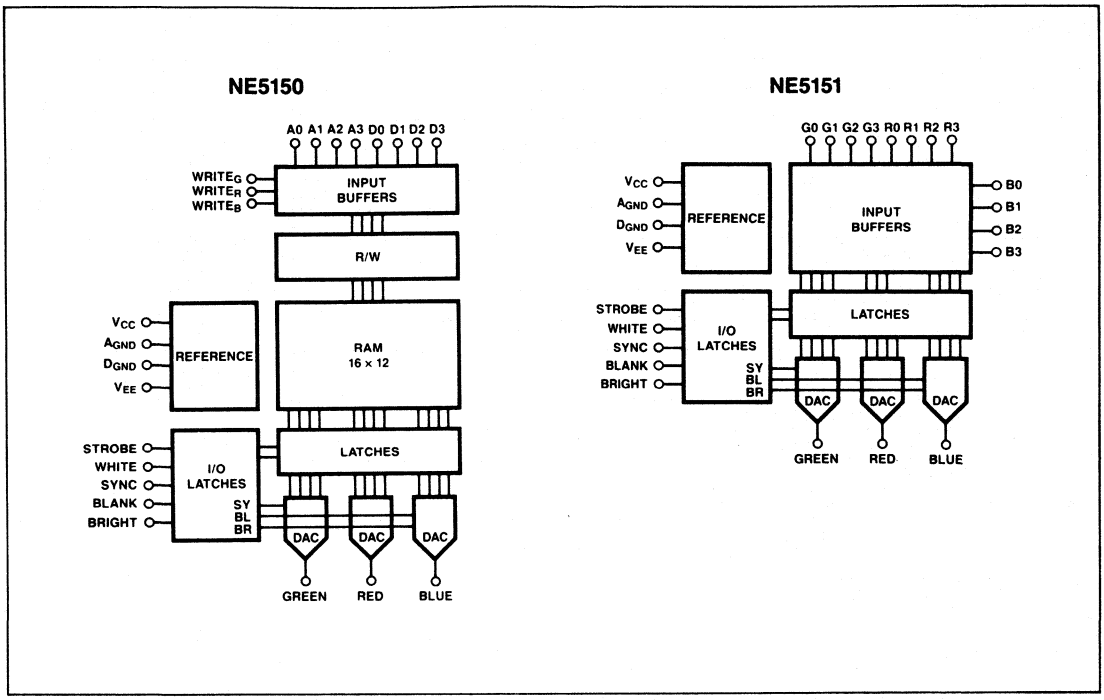


TOP VIEW
Order Number
NE5151F

Triple 4-Bit RGB DAC

NE5150/NE5151

BLOCK DIAGRAMS



4

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Temperature range		
Operating	0 to 70	°C
Storage	– 65 to 150	°C
Power supply		
V_{CC}	7.0	V
V_{EE}	– 7.0	V
Logic levels		
TTL-high	5.5	V
TTL-low	– 0.5	V
ECL-high	0.0	V
ECL-low	0 to V_{EE}	V

Triple 4-Bit RGB DAC NE5150/NE5151

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V (TTL), 0V (ECL), V_{EE} = −5V, 0°C < T_A < 70°C, unless otherwise noted.

SYMBOL	PARAMETER	LIMITS Min	Typ	Max	UNIT
	Resolution	4			bits
	Monotonicity	4			bits
NL	Nonlinearity		±1/16	±1/2	LSB
DNL	Differential nonlinearity		±1/8	±1	LSB
	Offset error (25°C) [1111] (BRT = 1)		±1/2	±1	LSB
	Gain error (25°C) [0000] (BRT = 1)		±1/2	±1	LSB
V_{CC}	Positive power supply (TTL mode) (ECL mode)	4.5 −0.1	5.0 0.0	5.5 0.1	V V
V_{EE}	Negative power supply (TTL or ECL mode)	−4.75	−5.0	−5.5	V
I_{CC}	Positive supply current		15	25	mA
I_{EE}	Negative supply current (NE5150) (NE5151)		175 145	210 175	mA mA
	Analog voltage range (ZS to FS)		603		mV
	Gain tracking (any two channels)			±1/4	LSB
	Least significant bit		40.2		mV
EWH	Enhanced white level absolute (25°C)		0		mV
BS	Bright shift (25°C) (0 to 1)		71.4		mV
EBL	Enhanced blanking level absolute (25°C)		−674		mV
ESY	Enhanced sync level absolute (25°C)		−960		mV
R_O	Output resistance (25°C)	67.5	75.0	82.5	Ω
V_{IH}	TTL logic input high	2.0			V
V_{IL}	TTL logic input low			0.8	V
I_{IH}	TTL logic high input current (V_{IN} = 2.4V)			20	μA
I_{IL}	TTL logic low input current (V_{IN} = 0.4V)			−1.6	mA
V_{IH}	ECL logic input high	−1.13			V
V_{IL}	ECL logic input low			−1.48	V
I_{IH}	ECL logic high input current (V_{IN} = −0.8V)			−1.0	mA
I_{IL}	ECL logic low input current (V_{IN} = −1.8V)			−1.0	mA

TEMPERATURE CHARACTERISTICS V_{CC} = 5V (TTL), 0V (ECL), V_{EE} = −5V, 0°C < T_A < 70°C

SYMBOL	PARAMETER	LIMITS Min	Typ	Max	UNIT
	Offset TC[1]			±100	ppm/°C
	Gain TC[1]			±200	ppm/°C
	Gain tracking TC (any two channels)			±50	ppm/°C
	Enhanced white level TC[1]			±100	ppm/°C
	Bright shift TC			±200	ppm/°C
	Enhanced blanking level TC			±300	ppm/°C
	Enhanced sync level TC			±300	ppm/°C
	Output resistance TC			+1000	ppm/°C

NOTE:
1. Normalized to full scale (603mV).

Triple 4-Bit RGB DAC

NE5150/NE5151

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V (TTL), 0V (ECL), V_{EE} = −5V, 0°C < T_A < 70°C

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
f_{MAX}	Maximum operating frequency (NE5150)	80			MHz
t_{WAS}	Write address setup (NE5150)		6		nsec
t_{WAH}	Write address hold (NE5150)		0		nsec
t_{WDS}	Write data setup (NE5150)		6		nsec
t_{WDH}	Write data hold (NE5150)		0		nsec
t_{WEW}	Write enable pulse width (NE5150)		6		nsec
t_{RCS}	Read composite[1] setup (NE5150)		4		nsec
t_{RCH}	Read composite[1] hold (NE5150)		2		nsec
t_{RAS}	Read address setup (NE5150)		8		nsec
t_{RAH}	Read address hold (NE5150)		0		nsec
t_{RSW}	Read strobe pulse width (NE5150)		8		nsec
t_{RDD}	Read DAC delay (NE5150)		8		nsec
f_{MAX}	Maximum operating frequency (NE5151)	150			MHz
t_{CS}	Composite[1] hold (NE5151)		4		nsec
t_{CH}	Composite[1] setup (NE5151)		2		nsec
t_{DS}	Data-bits setup (NE5151)		4		nsec
t_{DH}	Data-bits hold (NE5151)		2		nsec
t_{SW}	Strobe pulse width (NE5151)		4		nsec
t_{DD}	DAC delay (NE5151)		8		nsec
t_R	DAC rise time (10–90%)		3		nsec
t_S	DAC full-scale settling time[2]		10		nsec
C_{OUT}	Output capacitance (each DAC)		10		pF
S_R	Slew rate		200		V/μsec
G_E	Glitch energy			30	pV-sec
PSRR	Power supply rejection ratio (to red, green or blue outputs) V_{EE} at 1kHz V_{EE} at 10MHz V_{EE} at 50MHz V_{CC} at 1kHz V_{CC} at 10MHz V_{CC} at 50MHz		 43 28 14 80 50 36		 dB dB dB dB dB dB

NOTES:
1. Composite implies any of the WHITE, BRIGHT, BLANK or SYNC signals.
2. Settling to ± 1/2 LSB, measured from STROBE 50% point (rising edge). This time includes the delay through the strobe input buffer and latch.

4

Triple 4-Bit RGB DAC | NE5150/NE5151

PIN DESCRIPTION — NE5150

Write enable inputs use negative-true logic while all other inputs are positive-true. All inputs operate synchronously with the positive edge-triggered strobe input. When V_{CC} is taken high (5V), all inputs are TTL compatible. When V_{CC} is grounded, all inputs are ECL compatible. All DAC's are complementary, so that all ones is the highest absolute voltage and all zeroes is the lowest. All ones is called zero scale (ZS) and all zeroes is called fullscale (FS). The analog output voltage is approximately 0V (ZS) to −1V (SYNC).

Pins 1, 24, 23, 22: **DATA** bits D0 (MSB) through D3, used to input digital information to the memory during the write phase. During this phase, the data bits are presented to the internal latches (noninverted) and the DAC's will output the analog equivalent of the stored word, unless overridden by WHITE, BLANK or SYNC.

Pins 5, 4, 3, 2: **ADDRESS** lines A0 (MSB) through A3, used for selecting a memory address to write to or read from.

Pin 7: **WHITE** command. Presets the latches to all ones [1111] and outputs 0V absolute on all DAC's. Can be modified to −71mV absolute when BRIGHT is taken low. Will be overridden by either a BLANK or SYNC command.

Pin 8: **BRIGHT** command. A low input here turns on an additional −71mV (10 IRE unit) switch, shifting all other levels downward. Not overridden by any other input.

Pin 9: **BLANK** command. Presets the latches to all zeroes [0000] and turns on an additional −71mV (10 IRE unit) switch. Absolute output is −671mV. Can be modified another −71mV to −742mV absolute when BRIGHT is taken low. Will override WHITE, and will be overridden by SYNC.

Pin 10: **SYNC** command. Presets the latches to all zeroes [0000] and turns on the BLANK switch. Additionally turns on a −286mV (40 IRE unit) switch in the green channel only. Absolute output is −671mV for the red and blue channels, and −957mV for the green channel. All levels can be shifted −71mV by taking BRIGHT low. Overrides WHITE and BLANK.

Pins 11, 13, 15: **GREEN, RED, BLUE.** Analog outputs with 75-ohm internal termination resistors. Can directly drive 75-ohm cable and should be terminated at the display end of the line with 75 ohms. Output voltage range is approximately 0V to −1V independent of whether the digital inputs are ECL or TTL compatible. All outputs are simultaneously affected by the WHITE, BLANK, or BRIGHT commands. Only the GREEN channel carries SYNC information.

NOTE:
There are 100 IRE units from WHITE to BLANK. One IRE unit is approximately 7.1mV. Full scale is 90 IRE units and 10 IRE units is 1/9 of fullscale (e.g., BRIGHT function).

Pins 19, 20, 21: $\overline{\textbf{WRITE}_B}$, $\overline{\textbf{WRITE}_R}$, $\overline{\textbf{WRITE}_G}$. Write enable commands for each of the three 16 x 4 memories. When all write commands are high, then the *READ* operation is selected. This is the normal display mode. To write data into memory, the write enable pin is taken low. Data D0–D3 will be written into address A0–A3 of *each* memory when its corresponding write enable pin goes low.

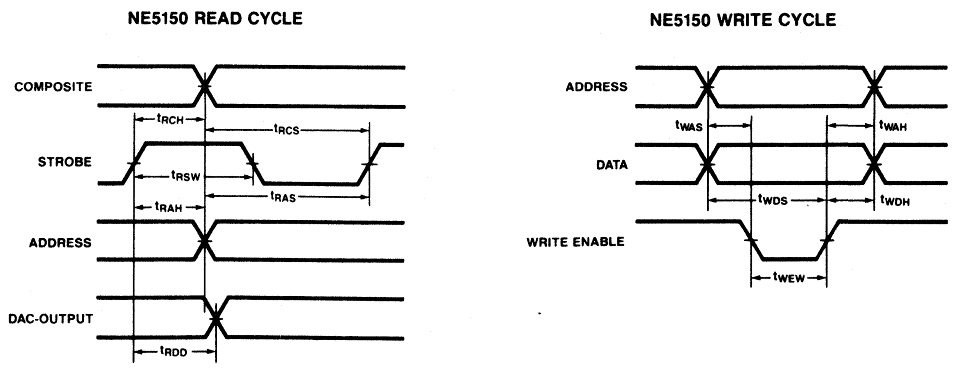
Pin 17: **STROBE.** The strobe signal is the main system clock and is used for resynchronizing digital signals to the DAC's. Preventing data skew eliminates glitches which would otherwise become visible color-distortions on a CRT display. The strobe command has no special drive requirements and is TTL or ECL compatible.

Pins 12, 16: $\mathbf{A_{GND}}$, $\mathbf{D_{GND}}$. Both **A**nalog and **D**igital ground carry a maximum of approximately 100mA of DC current. For proper operation, the difference voltage between A_{GND} and D_{GND} should be no greater than 50mV, preferably less.

Pin 14: $\mathbf{V_{EE}}$. The negative power supply is the main chip power source. V_{CC} is only used for the TTL input buffers. As is usual, good bypassing techniques should be used. The chip itself has a good deal of power supply rejection — well up into the VHF frequency range — so no elaborate power supply filtering is necessary.

Pin 18: **N/C.** This unused pin should be tied high or low.

NE5150 TIMING DIAGRAMS

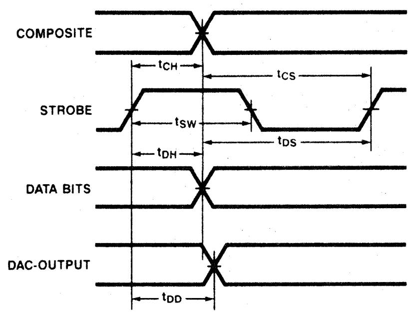


Triple 4-Bit RGB DAC NE5150/NE5151

NE5151 PIN DESCRIPTIONS AND TIMING DIAGRAM

The eleven digital inputs D0–D3, A0–A3, $\overline{\text{WRITE}}$ G/R/B, and the unused pin 18 of the NE5150 are replaced in the NE5151 with the three 4-bit DAC digital inputs G0–G3, R0–R3, and B0–B3. All other pin functions (e.g., composite functions, power supplies, strobe, etc.) are identical to the NE5150.

NE5151 TIMING

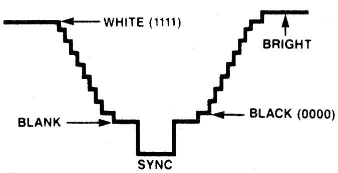


NE5150/NE5151 LOGIC TABLE

SYNC	BLANK	WHITE	BRIGHT	DATA	ADDRESS	OUTPUT	CONDITION
1	X	X	0	X	X	– 1031mV	SYNC[1]
1	X	X	1	X	X	– 960mV	Enhanced SYNC[1]
0	1	X	0	X	X	– 746mV	BLANK
0	1	X	1	X	X	– 674mV	Enhanced BLANK
0	0	1	0	X	X	– 71mV	WHITE
0	0	1	1	X	X	– 0mV	Enhanced WHITE
0	0	0	0	[0000]	Note 2	– 674mV	BLACK (FS)
0	0	0	1	[0000]	Note 2	– 603mV	Enhanced BLACK (EFS)
0	0	0	0	[1111]	Note 2	– 71mV	WHITE (ZS)
0	0	0	1	[1111]	Note 2	– 0mV	Enhanced WHITE (EZS)

NOTES
1. Green channel output only. RED and BLUE will output BLANK or Enhanced BLANK under these conditions.
2. For the NE5150 the DATA column represents the memory data accessed by the specific address. For the NE5151, the DATA is the direct digital inputs.

COMPOSITE VIDEO WAVEFORM



Selector Guide

COMPARATORS

DEVICE	COMPLEXITY	TEMP. RANGE*	MAX. INP. OFFSET VOLT (mV)	MAX. INP. CURRENT BIAS (μA)	MAX. INP. CURRENT OFFSET (μA)	SUPPLY VOLTAGE (V)	RESPONSE TIME (Typ.) (ns)	COMMON MODE VOLTAGE RANGE (V)	OUTPUT VOLTAGE V_{OL} Max. (V)	OUTPUT VOLTAGE V_{OH} Min. (V)	OUTPUT STRUCTURE	VOLTAGE GAIN (Typ.) V/mV	TTL FANOUT	MAX. DIFF. INPUT VOLTAGE (V)
LM111[1]	Single	M	4.00	0.15	0.02	±15	200	±14	0.4		O.C.	200	5	±30
LM211	Single	I	4.00	0.15	0.02	to	200	±14	0.4		O.C.	200	5	±30
LM311	Single	C	10.0	0.30	0.07	+5 and GND	200	±14	0.4		O.C.	200	5	±30
NE527[2]	Single	C	10.0	4.00	1.0	±5 to ±10	16	±5	0.5	2.7	TTL		5	±5
SE527	Single	M	6.00	4.00	1.00	and GND	16	±5	0.5	2.5	TTL		5	±5
NE529[5]	Single	C	10.0	50.0	15.0	±5 to ±10	12	±5	0.5	2.7	TTL		5	±5
SE529	Single	M	6.00	36.0	9.00	and GND	12	±5	0.5	2.5	TTL		5	±5
LM119[3]	Dual	M	7.00	1.00	0.10	±15	80	±13	0.4		O.C.	40	2	±5
LM219	Dual	I	7.00	1.00	0.10	to	80	±13	0.4		O.C.	40	2	±5
LM319	Dual	C	10.0	1.20	0.30	±5 and GND	80	±13	0.4		O.C.	40	2	±5
LM193[3]	Dual	M	9.00	0.30	0.10	±1 to ±18	1300	0 to $V_S - 2$	0.7		O.C.	200	2	36
LM293	Dual	I	9.00	0.40	0.15	or	1300	0 to $V_S - 2$	0.7		O.C.	200	2	36
LM393	Dual	C	9.00	0.40	0.15	+2 to +36 GND	1300	0 to $V_S - 2$	0.7		O.C.	200	2	36
LM2903	Dual	I	15.0	0.50	0.20		1300	0 to $V_S - 2$	0.7		O.C.	100	2	36
SE/NE521[4]	Dual	M/C	15/10.0	40.0	12.0	+5, −5, GND	8	±3	0.5	2.7	TTL		12	±6
SE/NE522	Dual	M/C	15/10.0	40.0	12.0	+5, −5, GND	10	±3	0.5		O.C.		12	±6
LM139[3]	Quad	M	9.00	0.30	0.10		1300	0 to $V_S - 2$	0.7		O.C.	200	2	36
LM239	Quad	I	9.00	0.40	0.15	±1 to ±18 or	1300	0 to $V_S - 2$	0.7		O.C.	200	2	36
LM339	Quad	C	9.00	0.40	0.15	+2 to +36	1300	0 to $V_S - 2$	0.7		O.C.	200	2	36
LM2901	Quad	I	15.0	0.50	0.20		1300	0 to $V_S - 2$	0.7		O.C.	100	2	36
MC3302[3]	Quad	I	40.0	1.00	0.30	+2 to +28 GND	2000	0 to $V_S - 2$	0.7		O.C.	100	2	28

Notes:
1. With strobe, will work from single supply.
2. Complementary output gates with individual strobes.
3. Will operate from single or dual supplies.
4. Ultra-high speed.

*Temperature Range
I = Industrial
C = Commercial
M = Military

Symbols and Definitions

Absolute Maximum Rating

Operating safe zones. Exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

BCD

Binary Coded Decimal.

$\overline{\text{BI}}$/RBO

Blanking Input or Ripple Blanking Output.

CE

Chip Enable.

CLR

Clear. Clear command will preset all internal circuits to a predetermined state.

Duty Cycle

Ratio of time on to time off. Generally expressed in percentage.

F_{MAX}

The maximum clock frequency: the maximum input frequency at a clock input for the predictable performance. Above this frequency the device may cease to function.

I_B

Input Bias Current. Current into an analog circuit input, specified at a particular voltage level.

I_{CC} ($-I_{CC}$)

Supply Current. The current flowing into the $+V_{CC}$ ($-V_{CC}$) supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.

I_{CEX}

Output Leakage Current. The current flowing out of or into a disabled (off) output with a specified High output voltage applied.

I_{IH}

Input High Current. The current flowing into or out of an input when a specified High level voltage is applied to that input.

I_{IL}

Input Low Current. The current flowing out of an input when a specified Low level voltage is applied to that input.

I_{OH}

Output Current Source the device can supply while maintaining a specified voltage output level.

I_{OL}

Output Low Current. The current flowing into an output when it is in the Low State.

I_{OS}

Output Short-Circuit Current. The current flowing out of an output which is in the High state when that output is shorted to ground.

I_S

Source Current. Current flowing into the V_S supply terminal of the device with specified operating conditions.

I_{SEG}

Segment Current. The amount of current supplied to each segment as a display. Current ratios are generally compared to segment 'b'.

LED

Light Emitting Diode.

Package Type Designation

See full package designations in Appendix.

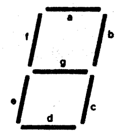
Power Dissipation

The power that the device can safely handle at 15°C. The dissipation must be derated as indicated for the individual package type.

$\overline{\text{RBI}}$

Ripple Blanking Input.

Segment Identification



T_A

Ambient temperature range. Allowable range of the surrounding environment of the operating device.

t_h

Hold Time. The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the current logic level may be released prior to the active transition of the timing pulse and still be recognized.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

t_{PHL}

Propagation Delay Times. The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{PLH}

Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{rec}

Recovery Time. The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_s

Setup Time. The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

Symbols and Definitions

DISPLAY DRIVER DEFINITIONS (Cont'd)

Truth Tables

0 is logic level low
1 is logic level high
X — don't care condition — has no effect under circuit conditions listed.

Typical Value

The typical value of a particular parameter at 25°C determined by characterization of the device or sampling. Usually indicates that the particular device is not 100% tested for the parameter because it does not vary or can be determined by design and other tested variables. Occasionally typical values are given rather than min-max values because 100% testing would raise the cost of the product to a prohibitive level. If a typical value must be guaranteed to ensure specific operation, custom testing can often be provided at an additional cost to the user.

V_{BR}

Output Breakdown Voltage. Maximum voltage applied to a disabled (off) output to ensure a leakage current less than the specified value.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

V_F

Forward voltage drop of a device at a specified current level.

V_{IH}

Input High Voltage. The range of input voltages recognized by the device as a logic high.

V_{IL}

Input Low Voltage. The range of input voltages recognized by the device as a logic low.

V_{IN}

The range of voltage on any input which the device can safely handle or a specified input voltage to the device.

V_{OH}

Output High Voltage. The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OL}

Output Low Voltage. The maximum guaranteed low voltage at an output terminal sinking the specified load current I_{OL}.

V_{OUT}

The range of voltage on any output which the device can safely handle or a specified output voltage to the device.

V_S

Source Voltage. A separate V_{CC} line depending on part type.

$\overline{XX}$

Negate Bar — when it appears over a function indicates that the "true" or valid condition of that function is a logic low level.
i.e. LE — would require a logic high level to cause a latch enable
$\overline{LE}$ — would require a logic low level to cause a latch enable.

Quad Line Driver
MC1488

DESCRIPTION

The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

FEATURES

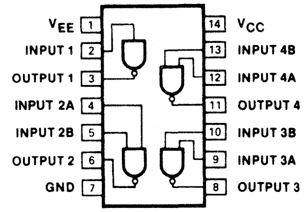
- **Current limited output: ±10mA Typ**
- **Power-off source impedance: 300Ω Min**
- **Simple slew rate control with external capacitor**
- **Flexible operating supply range**
- **Inputs are DTL/TTL compatible**

APPLICATIONS

- **Computer port driver**
- **Digital transmission over long lines**
- **Slew rate control**
- **TTL/DTL to MOS translation**

PIN CONFIGURATION

D,F,N PACKAGE



TOP VIEW

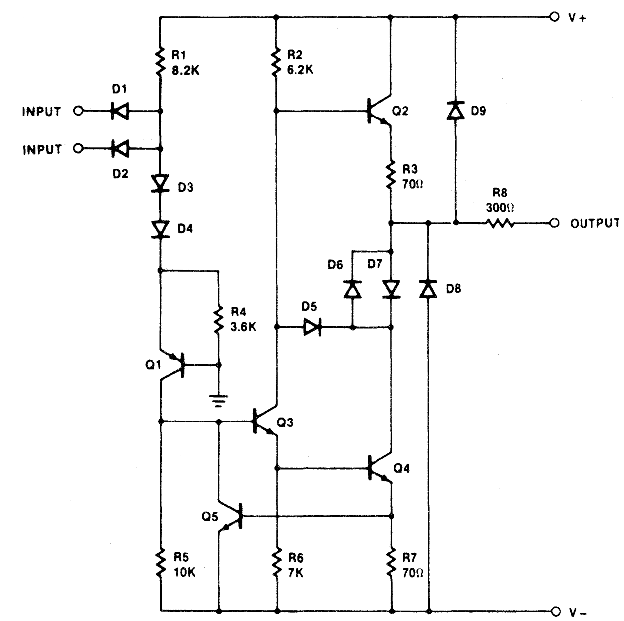
ORDER NUMBERS
MC1488D MC1488F, MC1488N

4

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage V+	+15	V
V-	-15	V
Input voltage (V_{IN})	$-15 \le V_{IN} \le 7.0$	V
Output voltage	±15	V
Power dissipation:		
F package	1000	mW
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10sec)	300	°C

CIRCUIT SCHEMATIC



1/4 CIRCUIT

Quad Line Driver | MC1488

DC ELECTRICAL CHARACTERISTICS

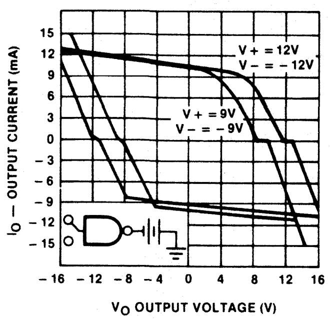
$V+ = +9.0V \pm 1\%$, $V- = -9.0V \pm 1\%$, $T_A = 0°C$ to $+75°C$ unless otherwise specified.
All typicals are for $V+ = 9.0V$, $V- = -9.0V$, and $T_A = 25°C$.*

PARAMETER	TEST CONDITIONS		LIMITS Min	Typ	Max	UNIT
Logic "0" input current	$V_{IN} = 0V$			-1.0	-1.6	mA
Logic "1" input current	$V_{IN} = +5.0V$			.005	10.0	μA
High level output voltage	$R_L = 3.0k\Omega$, $V_{IN} = 0.8V$	$V+ = 9.0V$, $V- = -9.0V$	6.0	7.0		V
		$V+ = 13.2V$, $V- = -13.2V$	9.0	10.5		V
Low level output voltage	$R_L = 3.0k\Omega$, $V_{IN} = 1.9V$	$V+ = 9.0V$, $V- = -9.0V$	-6.0	-6.8		V
		$V+ = 13.2V$, $V- = -13.2V$	-9.0	-10.5		V
High level output Short-circuit current	$V_{OUT} = 0V$, $V_{IN} = 0.8V$		-6.0	-10.0	-12.0	mA
Low level output Short-circuit current	$V_{OUT} = 0V$, $V_{IN} = 1.9V$		5.0	10.0	12.0	mA
Output resistance	$V+ = V- = 0V$, $V_{OUT} = \pm 2V$		300			Ω
Positive supply current (output open)	$V_{IN} = 1.9V$	$V+ = 9.0V$, $V- = -9.0V$		15.0	20.0	mA
		$V+ = 12V$, $V- = -12V$		19.0	25.0	mA
		$V+ = 15V$, $V- = -15V$		25.0	34.0	mA
	$V_{IN} = 0.8V$	$V+ = 9.0V$, $V- = -9.0V$		4.5	6.0	mA
		$V+ = 12V$, $V- = -12V$		5.5	7.0	mA
		$V+ = 15V$, $V- = -15V$		8.0	12.0	mA
Negative supply current (output open)	$V_{IN} = 1.9V$	$V+ = 9.0V$, $V- = -9.0V$		-13.0	-17.0	mA
		$V+ = 12V$, $V- = -12V$		-18.0	-23.0	mA
		$V+ = 15V$, $V- = -15V$		-25.0	-34.0	mA
	$V_{IN} = 0.8V$	$V+ = 9.0V$, $V- = -9.0V$		-1	-15	μA
		$V+ = 12V$, $V- = -12V$		-1	-15	μA
		$V+ = 15V$, $V- = -15V$		-.01	-2.5	mA
Power dissipation	$V+ = 9.0V$, $V- = -9.0V$			252	333	mW
	$V+ = 12V$, $V- = -12V$			444	576	mW
Propagation delay to "1" (t_{pd1})	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			275	560	ns
Propagation delay to "0" (t_{pd0})	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			70	175	ns
Rise time (t_r)	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			75	100	ns
Fall time (t_f)	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			40	75	ns

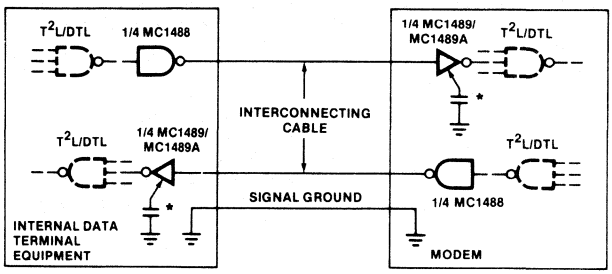
NOTE
*Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS



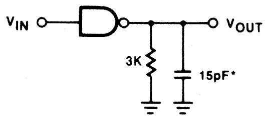
RS232C DATA TRANSMISSION



NOTE

*Optional for noise filtering

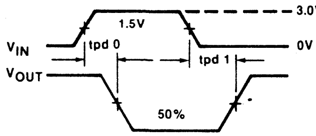
AC LOAD CIRCUIT



NOTE

*C_L includes probe and jig capacitance.

SWITCHING WAVEFORMS



NOTE

t_r and t_f are measured between 10% and 90% of the output waveform

APPLICATIONS

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

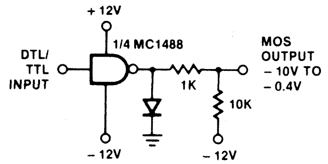
$$C = I_{SC} (\Delta T / \Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V / \Delta T$ is the slew rate.

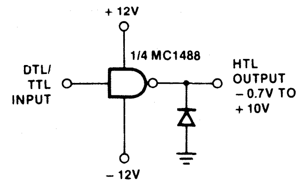
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

TYPICAL APPLICATIONS

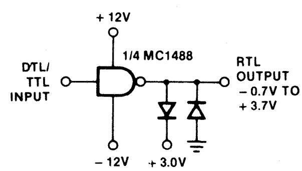
DTL/TTL-TO-MOS TRANSLATOR



DTL/TTL-TO-HTL TRANSLATOR



DTL/TTL-TO-RTL TRANSLATOR



Quad Line Receivers

MC1489/MC1489A

DESCRIPTION

The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C.

FEATURES

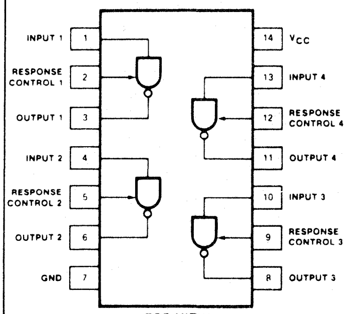
- **Four totally separate receivers per package**
- **Programmable threshold**
- **Built-in input threshold hysteresis**
- **"Fail safe" operating mode**
- **Inputs withstand ±30V**

APPLICATIONS

- **Computer port inputs**
- **Modems**
- **Eliminating noise in digital circuitry**
- **MOS to TTL/DTL translation**

PIN CONFIGURATION

D, F, N PACKAGE

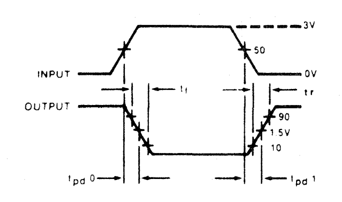


TOP VIEW
ORDER NUMBERS
MC1489D, MC1489AD
MC1489F, MC1489AF, MC1489N, MC1489AN

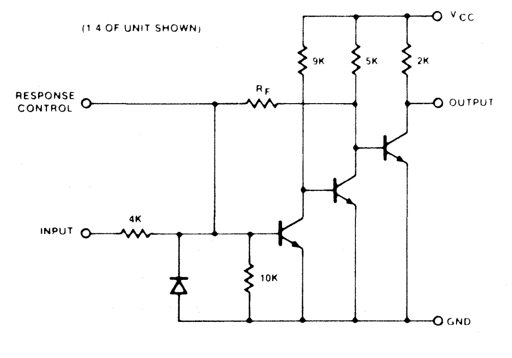
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage	10	V
Input voltage range	±30	V
Output load current	20	mA
Power dissipation		
F package	1	W
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C

VOLTAGE WAVEFORMS

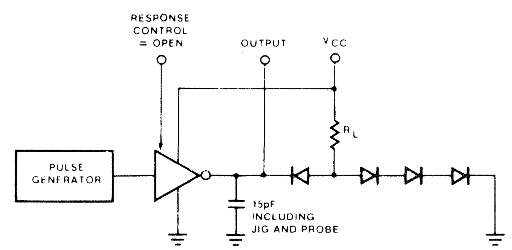


EQUIVALENT SCHEMATIC



MC1489: R_F = 10k
MC1489A: R_F = 2k

AC TEST CIRCUIT



Quad Line Receivers MC1489/MC1489A

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 1%, 0°C ≤ T_A ≤ +75°C unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	MC1489 Min	MC1489 Typ	MC1489 Max	MC1489A Min	MC1489A Typ	MC1489A Max	UNIT
Input high threshold voltage	T_A = 25°C, V_{OUT} ≤ 0.45V, I_{OUT} = 10mA	1.0		1.5	1.75		2.25	V
Input low threshold voltage	T_A = 25°C, V_{OUT} ≤ 2.5V, I_{OUT} = -0.5mA	0.75		1.25	0.75		1.25	V
	V_{IN} = +25V	+3.6	+5.6	+8.3	+3.6	+5.6	+8.3	mA
	V_{IN} = -25V	-3.6	-5.6	-8.3	-3.6	-5.6	-8.3	mA
Input current	V_{IN} = +3V	+0.43	+0.53		+0.43	+0.53		mA
	V_{IN} = -3V	-0.43	-0.53		-0.43	-0.53		mA
Output high voltage	V_{IN} = 0.75V, I_{OUT} = -0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
	Input = Open, I_{OUT} = -0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
Output low voltage	V_{IN} = 3.0V, I_{OUT} = 10mA		0.33	0.45		0.33	0.45	V
Output short circuit current	V_{IN} = 0.75V		3.0			3.0		mA
Supply current	V_{IN} = 5.0V		20	26		20	26	mA
Power dissipation	V_{IN} = 5.0V		100	130		100	130	mW

NOTES
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

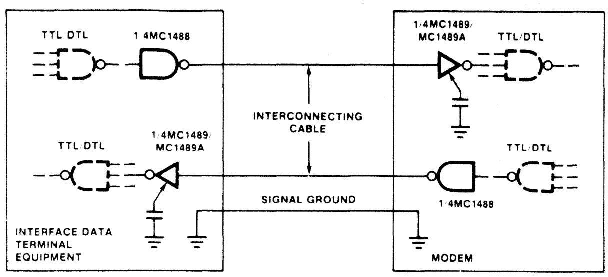
AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 1%, T_A = 25°C unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	MC1489 Min	MC1489 Typ	MC1489 Max	MC1489A Min	MC1489A Typ	MC1489A Max	UNIT
Input to output "high" Propagation delay (t_{pd1})	R_L = 3.9kΩ (AC test circuit)		25	85		25	85	ns
Input to output "low" Propagation delay (t_{pd0})	R_L = 390Ω (AC test circuit)		20	50		20	50	ns
Output rise time	R_L = 3.9kΩ (AC test circuit)		110	175		110	175	ns
Output fall time	R_L = 390Ω (AC test circuit)		9	20		9	20	ns

NOTES
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

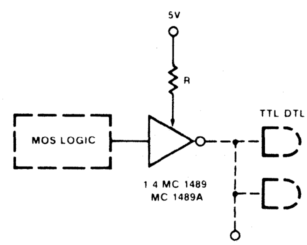
TYPICAL APPLICATIONS

RS232C DATA TRANSMISSION



*Optional for noise filtering

MOS TO TTL/DTL TRANSLATOR



4

Addressable Relay Driver NE5090

DESCRIPTION

The NE5090 addressable relay driver is a high current latched driver, similar in function to the 9934 address decoder. The device has 8 open collector Darlington power outputs, each capable of 150mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3 bit address. The device must be enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$, turns all outputs off when a logic "0" is applied. The device is packaged in a 16 pin plastic or CERDIP package.

FEATURES

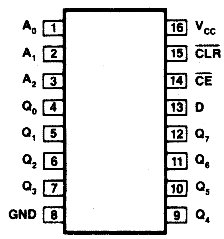
- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **Will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **Pin compatible with 9334**

APPLICATIONS

- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATION

D[1],F,N PACKAGE

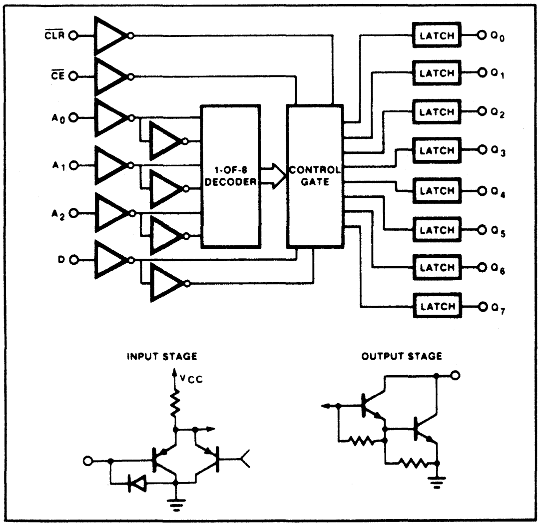


TOP VIEW

ORDER NUMBERS
NE5090N
NE5090F
NE5090D[1]

NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage	−0.5 to +15	V
V_{OUT}	Output voltage	0 to +30	V
I_{GND}	Ground current	500	mA
I_{OUT}	Output current Each output	200	mA
P_D	Power dissipation[1]	1	W
Ambient temperature range			°C
T_A	NE5090	0 to +70	
T_J	Junction	150	
T_{STG}	Storage	−65 to +150	
T_{sold}	Lead soldering temperature (10 sec max)	300	°C

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1-3	A0-A2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	Q0-Q7	The 8 device outputs.
13	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF"
14	CE	The chip enable. When this input is low, the output latches will accept data. When CE goes high, all outputs will retain their existing state, regardless of address of data input conditions.
15	CLR	The clear input. When CLR goes low all output switches are turned "OFF". The high data input will override the clear function on the addressed latch.

TRUTH TABLE

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	H	Q_{N-1} →							Addressable Latch
H	L	H	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1} →							H	
H	L	H	H	H	H	Q_{N-1} →							L	

X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"ON" output state
H = High voltage level/"OFF" output state

DC ELECTRICAL CHARACTERISTICS V_{CC} = 4.75V to 5.25V, 0°C ≤ T_A ≤ 70°C unless otherwise specified (NE5090)[2].

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
 V_{IH} V_{IL}	Input voltage High Low		 2.0		 0.8	V
V_{OL}	Output voltage Low	 I_{OL} = 150mA, T_A = 25°C Over temperature		 1.05	 1.30 1.50	V
 I_{IH} I_{IL}	Input current High Low	 $V_{IN} = V_{CC}$ V_{IN} = 0V		 < 1.0 −3.0	 10 −250	μA
I_{OH}	Leakage current	V_{OUT} = 28V,		5	250	μA
 I_{CCL} I_{CCH}	Supply current All outputs low All outputs high	V_{CC} = 5.25V NE5090		 35 22	 60 50	mA

NOTES

1. Derate power dissipation as indicated above threshold ambient temperature
   NE5090 N at 9.3mW/°C above 85°C
   NE5090 F at 7.5mW/°C above 65°C
2. All typical values are at V_{CC} = 5V and T_A = 25°C

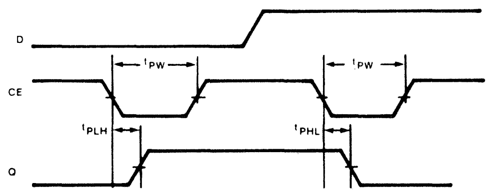
SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$, $V_{OUT} = 5V$, $I_{OUT} = 100mA$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$

PARAMETER		TO	FROM	Min	Typ	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay time Low to high[1] High to low[1]	Output	$\overline{CE}$		900 130	1800 260	ns
t_{PLH} t_{PHL}	Low to high[2] High to low[2]	Output	Data		920 130	1850 260	ns
t_{PLH} t_{PHL}	Low to high[3] High to low[3]	Output	Address		900 130	1800 260	ns
t_{PLH} t_{PHL}	Low to high[4] High to low[4]	Output	$\overline{CLR}$		920	1850	ns
SWITCHING SETUP REQUIREMENTS							
$t_{s(H)}$[5] $t_{s(L)}$[5]		Chip enable Chip enable	High data Low data	5 10	20 30		ns
$t_{s(A)}$[6]		Chip enable	Address	0	20		ns
$t_{h(H)}$[5] $t_{H(L)}$[5]		Chip enable Chip enable	High data Low data	+ 10 + 10	0 0		ns
$t_{pw(E)}$[1]	Chip enable pulse width[1]			0	20		ns

NOTES
1. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
4. See Turn-Off Delay, Clear to Output timing diagram.
5. See Setup and Hold Time, Data to Enable timing diagram.
6. See Setup Time, Address to Enable timing diagram.

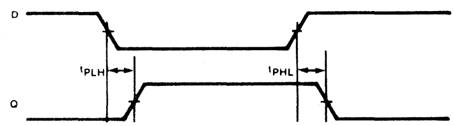
TIMING DIAGRAMS

TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



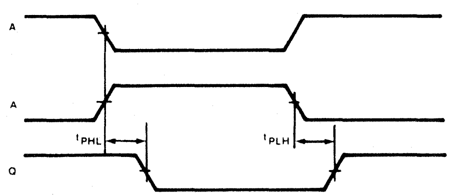
Other Inputs: $\overline{CLR}$ = H, A = Stable.

TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



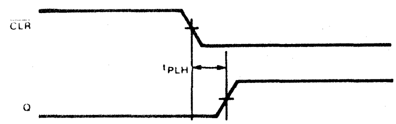
Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = H, A = Stable

TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

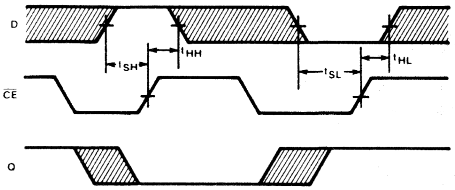
TURN-OFF DELAY, CLEAR TO OUTPUT



Other Inputs: $\overline{CE}$ = H.

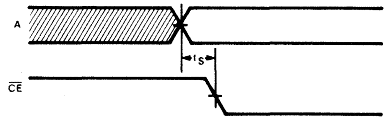
TIMING DIAGRAMS (Cont'd)

SETUP AND HOLD TIME, DATA TO ENABLE



Other Inputs: $\overline{CLR}$ = H. A = Stable.

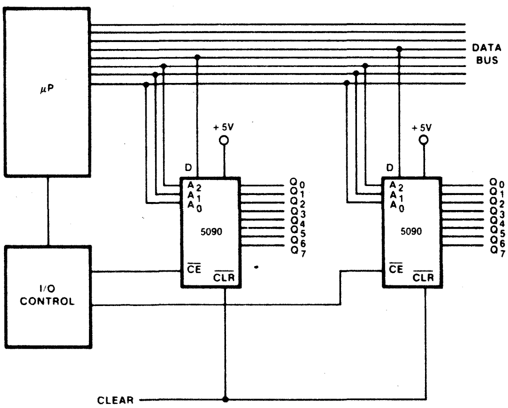
SETUP TIME, ADDRESS TO ENABLE



Other Inputs: $\overline{CLR}$ = H.

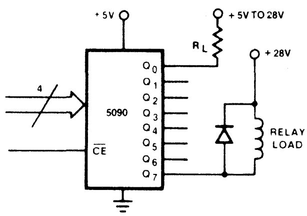
TYPICAL APPLICATIONS

INTERFACING WITH A MICROPROCESSOR SYSTEM

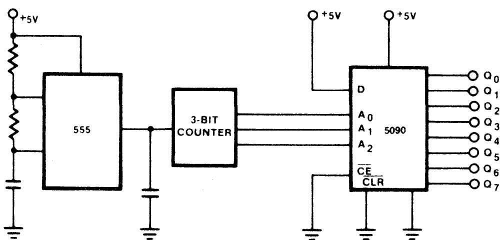


A_0, A_1, A_2, may be connected to the address bus if permitted by system design.

DRIVING SIMPLE LOADS



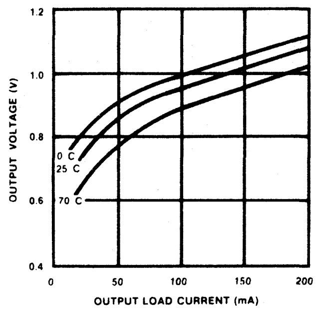
OPERATING IN DEMULTIPLEX MODE



4

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE VS LOAD CURRENT



Octal Line Driver

NE5170

DESCRIPTION

The NE5170 is an octal line driver which is designed for digital communications with data rates up to 100Kb/s. This device meets all the requirements of EIA standards RS232C/RS423A and CCITT recommendations V.10/X.26. Three programmable features, (1) output slew rate (2) output voltage level, and (3) three-state control (high impedance) are provided so that output characteristics may be modified to meet the requirements of specific applications.

FEATURES

- **Meets EIA RS232C/423A and CCITT V.10/X.26**
- **Simple slew rate programming with a single external resistor**
- **0.1 to 10V/μs slew rate range**
- **High/low programmable voltage output modes**
- **TTL compatible inputs**

APPLICATIONS

- **High speed modems**
- **High speed parallel communications**
- **Computer I/O ports**
- **Logic level translation**

FUNCTION TABLE

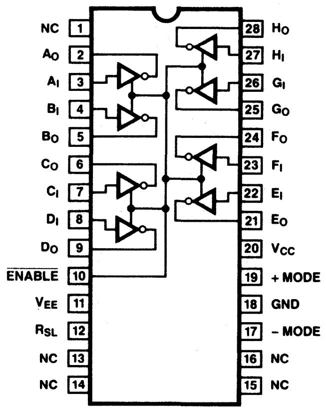
$\overline{\text{ENABLE}}$	LOGIC INPUT	OUTPUT VOLTAGE (V)		
		RS423A[1]	RS232C	
			Low Output Mode[1]	High Output Mode[2]
L	L	5 to 6V	5 to 6V	≥ 9V
L	H	−5 to −6V	−5 to −6V	≤ −9V
H	X	High Z	High Z	High Z

NOTES:

1. V_{CC} = +10V and V_{EE} = −10V; R_L = 3KΩ
2. V_{CC} = +12V and V_{EE} = −12V; R_L = 3KΩ

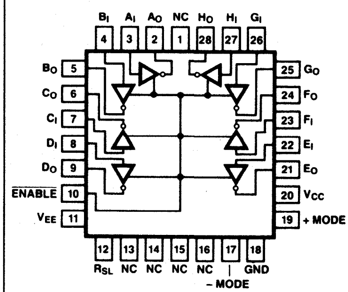
PIN CONFIGURATION

N Package



TOP VIEW
Order Number
NE5170N

G Package



TOP VIEW
Order Number
NE5170G

Octal Line Driver — NE5170

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Supply Voltage V_{CC}	15	V
Supply Voltage V_{EE}	−15	V
Output Current[1]	±150	mA
Input Voltage ($\overline{Enable}$, Data)	−1.5 to +7	V
Output Voltage[2]	+15	V
Minimum Slew Resistor[3]	1K	Ω
Power Dissipation	800	mW

DC ELECTRICAL CHARACTERISTICS V_{CC} (see notes 4, 5), $0°C \leq T_A \leq 70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNITS
			Min	Max	
V_{OH}	Output high voltage	$V_{IN} = 0.8V$, $R_L = 3K\Omega^4$	5	6	V
		$R_L = 450\Omega^4$	4.5	6	
		$R_L = 3K\Omega^5$, $C_L = 2500pF$	$V_{CC} - 3$		
V_{OL}	Output low voltage	$V_{IN} = 2.4V$, $R_L = 3K\Omega^4$	−6	−5	V
		$R_L = 450\Omega^4$	−6	−4.5	
		$R_L = 3K\Omega^5$, $C_L = 2500pF$		$V_{EE} + 3$	
	Output unbalance voltage	$V_{CC} = \|V_{EE}\|$, $R_L = 450\Omega^4$		0.4	V
I_{CEX}	Output leakage current	$\|V_O\| = 6V$, ENABLE = 2V or $V_{CC} = V_{EE} = 0V$	−100	100	μA
V_{IH}	Input high voltage		2.0		V
V_{IL}	Input low voltage			0.8	V
I_{IL}	Logic "0" input current	$V_{IN} = 0.4V$	−400	0	μA
I_{IH}	Logic "1" input current	$V_{IN} = 2.4V$	0	40	μA
I_{OS}	Output short circuit current	$V_O = 0V$	−150	150	μA
V_{CL}	Input clamp voltage	$I_{IN} = -15mA$	−1.5		V
I_{CC}	Supply current	NO LOAD		40	mA
I_{EE}		NO LOAD	−40		mA

NOTES:
1. Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.
2. High impedance mode.
3. Minimum value of the resistor used to set the slew rate.
4. V_{OH}, V_{OL} at $R_L = 450\Omega$ will be $\geq 90\%$ of V_{OH}, V_{OL} at $R_L = \infty$.
5. High Output Mode; +MODE pin = V_{CC}; −MODE pin = V_{EE}; $9V \leq V_{CC} \leq 13V$; $-9V \geq V_{EE} \geq -13V$.

Octal Line Driver

NE5170

AC ELECTRICAL CHARACTERISTICS $V_{CC} = +10V$; $V_{EE} = -10V$; Mode = GND, $0°C \leq T_A \leq 70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Max	UNITS
t_{PHZ}	Propagation delay output high to high impedance	$R_L = 450$, $C_L = 50pF$ or $R_L = 3K$, $C_L = 2500pF$		5	μs
t_{PLZ}	Propagation delay output low to high impedance	$R_L = 450$, $C_L = 50pF$ or $R_L = 3K$, $C_L = 2500pF$		5	μs
t_{PZH}	Propagation delay high impedance to high output	$R_{SL} = 200K$ $R_L = 450$, $C_L = 50pF$ or $R_L = 3K$, $C_L = 2500pF$		150	μs
t_{PZL}	Propagation delay high impedance to low output	$R_{SL} = 200K$ $R_L = 450$, $C_L = 50pF$ or $R_L = 3K$, $C_L = 2500pF$		150	μs
SR	Ouput slew rate[1]	$R_{SL} = 2K \pm 1\%$	8	12	V/μs
		$R_{SL} = 20K \pm 1\%$	0.8	1.2	
		$R_{SL} = 200K \pm 1\%$	0.073	0.127	

NOTE:
1. SR: Load condition. (A) For $R_{SL} < 4K\Omega$ use $R_L = 450\Omega$; $C_L = 50pF$; (B) For $R_{SL} > 4K\Omega$ use either $R_L = 450\Omega$, $C_L = 50pF$ or $R_L = 3K\Omega$, $C_L = 2500pF$.

SLEW RATE PROGRAMMING

Slew rate for the NE5170 is set using a single external resistor connected between the R_{SL} pin and ground. Adjustment is made according to the formula:

$$R_{SL} \text{ (in kilohms)} = \frac{20}{\text{Slew Rate}}$$

where the slew rate is in V/μs. The slew resistor can vary between 2 and 200 kilohms which gives a slew rate range of 10 to 0.1V/μs. This adjustment of the slew rate allows tailoring output characteristics to recommendations for cable length and data rate found in EIA standard RS423A. Approximations for cable length and data rate are given by:

Max. data rate (in Kb/s) = 300/t

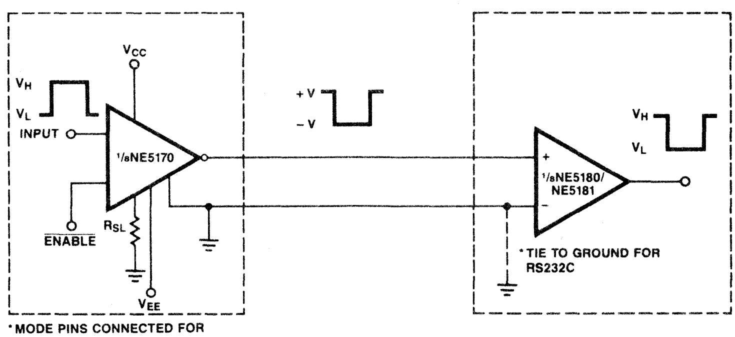
Cable length (in feet) = 100 x t

where t is the rise time in microseconds. The absolute maximum data rate is 100Kb/s and the absolute maximum cable length is 4000 feet.

OUTPUT MODE PROGRAMMING

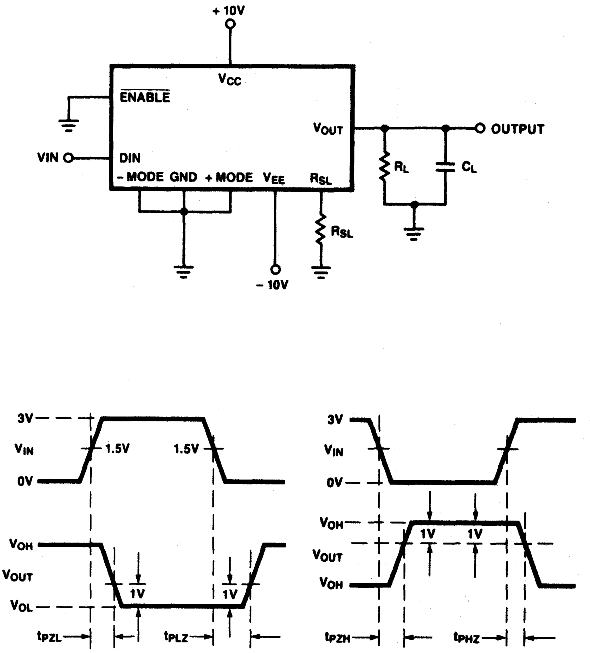
The NE5170 has two programmable output modes which provide different output voltage levels. The low output mode meets the specifications of EIA standards RS423A and RS232C. The high output mode meets the specifications of RS232C only since higher output voltages result from programming this mode. The high output mode provides the greater output voltages where higher attenuation levels must be tolerated. Programming the high output mode is accomplished by connecting the +MODE pin to V_{CC} and the −MODE pin to V_{EE}. The low output mode results when both of these pins are connected to ground.

APPLICATIONS



RS232C/RS423A Data Transmission

AC PARAMETER TEST CIRCUIT AND WAVEFORMS



NOTES: 1) See AC electrical characteristics table for values of R_{SL}, R_L and C_L.
2) V_{IN} pulse: Frequency = 1kHz, duty cycle = 50%, Z_{OUT} = 50Ω, $t_r = t_f \leq 10ns$.

Octal Line Receivers

NE5180/NE5181

DESCRIPTION

The NE5180 and NE5181 are octal line receivers designed to interface data terminal equipment with data communications equipment. These devices meet the requirements of EIA standards RS232C, RS423A, RS422A, and CCITT V.10, V.11, V.28, X.26 and X.27. The NE5180 is intended for use where the data transmission rate is up to 200 Kb/s. The NE5181 covers the entire range of data rates up to 10 Mb/s. The difference in data rates for the two devices results from the input filtering of the NE5180. These devices also provide a failsafe feature which protects against certain input fault conditions.

FEATURES

- **Meets EIA RS232C/423A/422A and CCITT V.10, V.11, V.28**
- **Single +5V supply — TTL compatible outputs**
- **Differential inputs withstand ±25V**
- **Failsafe feature**
- **Input noise filter (NE5180 only)**
- **Internal hysteresis**

APPLICATIONS

- **High speed modems**
- **High speed parallel communications**
- **Computer I/O ports**
- **Logic level translation**

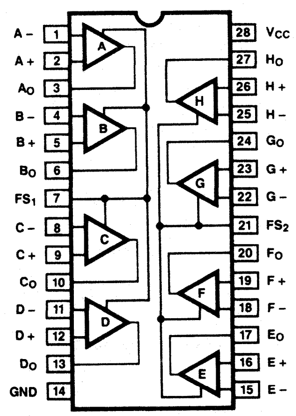
FUNCTION TABLE

INPUT	FAILSAFE INPUT	LOGIC OUTPUT
$V_{ID} > 200$ mV[1]	X	H
$V_{ID} < -200$mV[1]	X	L

NOTE:
1. V_{ID} is defined as the non-inverting terminal input voltage minus the inverting terminal input voltage.

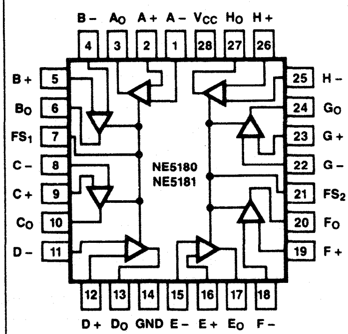
PIN CONFIGURATION

N Package



TOP VIEW
Order Numbers
NE5180N NE5181N

G Package



TOP VIEW
Order Numbers
NE5180G NE5181G

Octal Line Receivers

NE5180/NE5181

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Power Dissipation	800	mW
Supply Voltage (V_{CC})	7	V
Common Mode Range	±15	V
Differential Input Voltage (V_{ID})	±25	V
Output Sink Current	50	mA
Failsafe Voltage	−0.3 to V_{CC}	V
Output Short Circuit Time	1	sec

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ T_A ≤ 70°C, input common mode range ±7V

SYMBOL	PARAMETER	TEST CONDITIONS		NE5180		NE5181		UNITS
				Min	Max	Min	Max	
R_{IN}	DC input resistance	$3V \le \lvert V_{IN} \rvert \le 25V$		3K	7K	3K	7K	Ω
V_{OFS}	Failsafe output voltage	Inputs open or shorted together	$0 \le I_{OUT} \le 8mA$, $V_{failsafe} = 0V$		0.45		0.45	V
			$0 \ge I_{OUT} \ge -400\mu A$, $V_{failsafe} = V_{CC}$	2.7		2.7		
V_{th}	Differential input high[4] threshold	$V_{OUT} = 2.7V$, $I_{OUT} = -440\mu A$	$R_S = 0$[1]		0.2		0.2	V
			$R_S = 500$[1]		0.4		0.4	
V_{tl}	Differential input low[4] threshold	$V_{OUT} = 0.45V$, $I_{OUT} = 8mA$	$R_S = 0$[1]	−0.2		−0.2		V
			$R_S = 500$[1]	−0.4		−0.4		
V_H	Hysteresis[4]	$F_S = 0V$ or V_{CC} (See Figure 1)		60	140	60	140	mV
V_{IOC}	Open circuit input voltage				2		2	V
C_I	Input capacitance				100		100	pF
V_{OH}	High level output voltage	$V_{ID} = 1V$, $I_{OUT} = -440\mu A$		2.7		2.7		V
V_{OL}	Low level output voltage	$V_{ID} = -1V$	$I_{OUT} = 4mA$[2]		0.4		0.4	V
			$I_{OUT} = 8mA$[2]		0.45		0.45	
I_{OS}	Short circuit output current	Note 3		20	100	20	100	mA
I_{CC}	Supply current	$4.75V \le V_{CC} \le 5.25V$			125		125	mA
I_{IN}	Input current	Other inputs grounded	$V_{IN} = +10V$		3.25		3.25	mA
			$V_{IN} = -10V$	−3.25		−3.25		

NOTES:
1. R_S is a resistor in series with each input.
2. Measured after 100ms warm up (at 0°C).
3. Only 1 output may be shorted at a time and then only for a maximum of 1 sec.
4. See Figure 1 for threshold and hysteresis definitions.

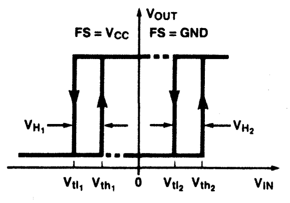


Figure 1. V_{tl}, V_{th}, V_H Definition

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ T_A ≤ 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	NE5180		NE5181		UNITS
			Min	Max	Min	Max	
t_{PLH}	Propagation delay — low to high	$C_L = 50pF$, $V_{IN} = \pm 1V$		300		70	ns
t_{PHL}	Propagation delay — high to low	$C_L = 50pF$, $V_{IN} = \pm 1V$		300		70	ns
f_a	Acceptable input frequency	Unused input grounded, $V_{IN} = \pm 200mV$		0.1		5.0	MHz
f_r	Rejectable input frequency	Unused input grounded, $V_{IN} = \pm 500mV$	5.5		NA		MHz

Octal Line Receivers

NE5180/NE5181

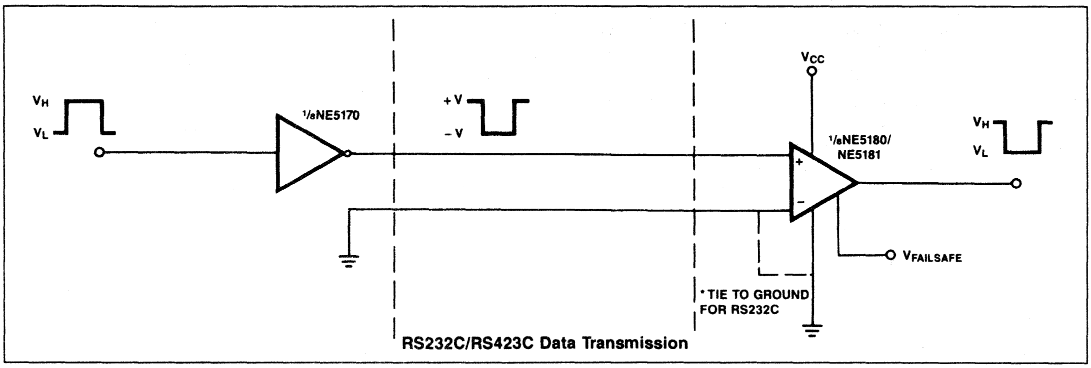
FAILSAFE OPERATION

These devices provide a failsafe operating mode to guard against input fault conditions as defined in RS422A and RS423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to V_{CC} provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the NE5180 or NE5181 where each provides common failsafe control for four receivers.

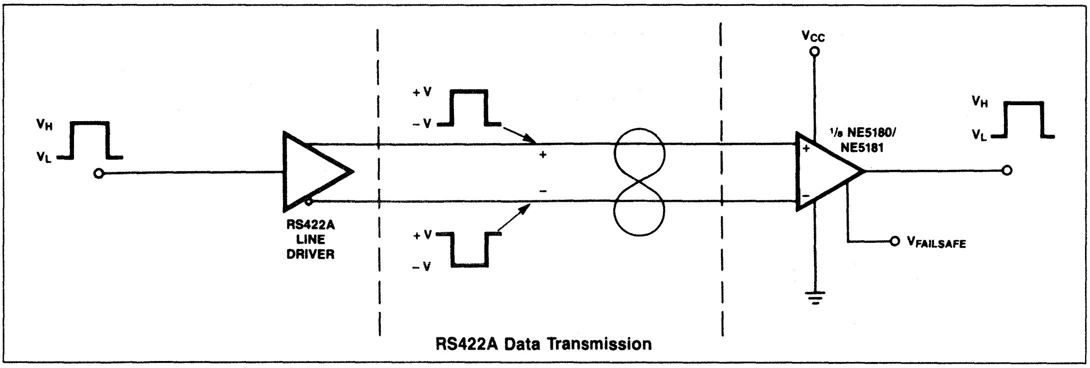
INPUT FILTERING (NE5180)

The NE5180 has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5MHz at ±500mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output. As the signal amplitude decreases (increases) the rejected frequency decreases (increases).

APPLICATIONS

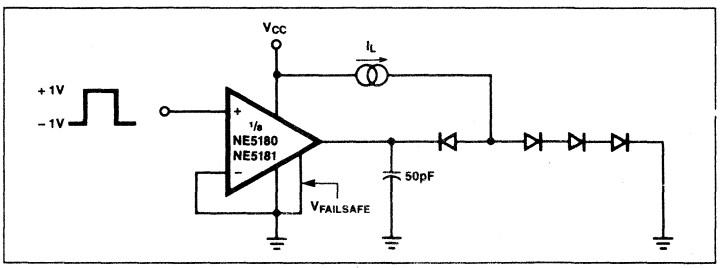


RS232C/RS423C Data Transmission

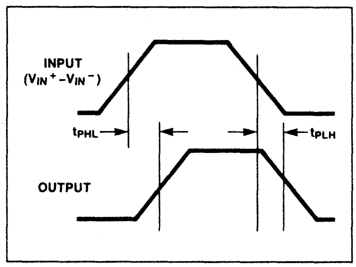


RS422A Data Transmission

AC TEST CIRCUIT



VOLTAGE WAVEFORMS



LED Decoder/Driver | NE587

DESCRIPTION

The NE587 is a latch/decoder/driver for 7-segment common anode LED displays. The NE587 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

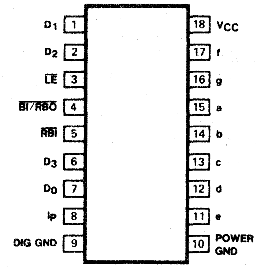
- **Latched BCD inputs**
- **Low loading bus-compatible inputs**
- **Ripple-blanking on leading and/or trailing edge zeros**

APPLICATIONS

- **Digital panel meters**
- **Measuring instruments**
- **Test equipment**
- **Digital clocks**
- **Digital bus monitoring**

PIN CONFIGURATIONS

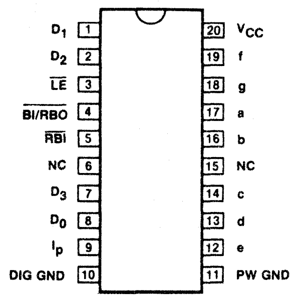
F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE587F NE587N

D2 PACKAGE



TOP VIEW
NE587D[2]

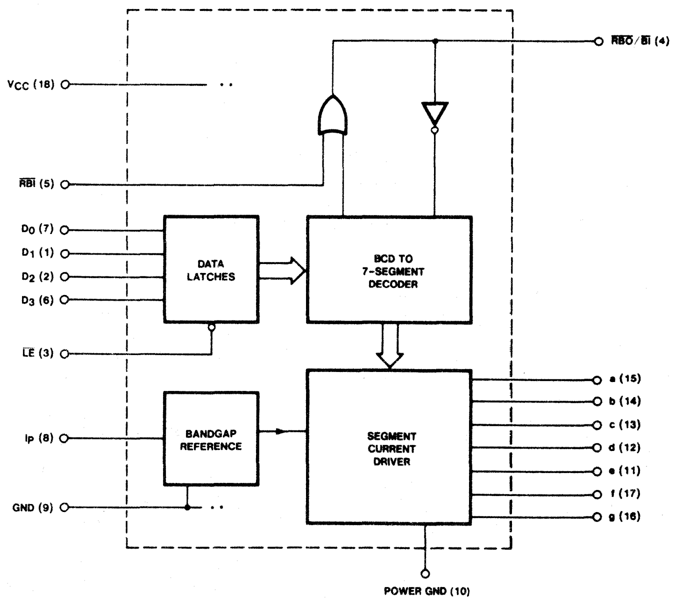
NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage (D_0 - D_3, $\overline{LE}$, $\overline{RBI}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a-g, RBO)	−0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Soldering temperature (10 sec. max)	300	°C

NOTE
Derate power dissipation as indicated
N package - 95°C/watt above 55°C
F package - 100°C/watt above 50°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C < T_A < 70°C.
Typical values are at V_{CC} = 5V, T_A = 25°C, R_P = 1kΩ (± 1%) unless otherwise stated.

PARAMETER		TEST CONDITIONS	NE587			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All Inputs except $\overline{BI}$ $\overline{BI}$	2.0 2.0		15 5.5	V
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	I_{IN} = −12mA, T_A = 25°C			−1.5	V
I_{IH}	Input high current	Inputs D_0 −D_3, $\overline{LE}$, $\overline{RBI}$ V_{IN} = 2.4V V_{IN} = 15V Input $\overline{BI}$ (pin 4) $\overline{RBI}$ = H V_{IN} = V_{CC} = 5.25V		 1.0 15 10	 10 15 100	µA µA
I_{IL}	Input low current	V_{IN} = 0.4V, Inputs D_0 − D_3 $\overline{LE}$, $\overline{RBI}$ Input $\overline{BI}$ V_{CC} = 5.25V $\overline{RBI}$ = H, V_{IN} = 0.4V		−5 −200 −0.7		µA mA
V_{OL}	Output low voltage	Output $\overline{RBO}$ I_{out} = 3.0mA		.2	.5	V
V_{OH}	Output high voltage	Output $\overline{RBO}$ I_{OUT} = −50µA $\overline{RBI}$ = H	3.5	4.5		V
I_{OUT}	Output segment "ON" current	Outputs "a" thru "g" V_{OUT} = 2.0V	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment V_{OUT} = 2.0V	0.90	1.00	1.10	
I_{OFF}	Output segment "OFF" current	Outputs "a" thru "g" V_{OUT} = 5.0V		20	250	µA
I_{CCO}	Supply current	V_{CC} = 5.25V All outputs "ON" V_{OUT} > 1V		33	55	mA
I_{CCI}	Supply current	V_{CC} = 5.25V All outputs blanked		50	70	mA

NOTE
NE587 PROGRAMMING
The NE587 output current can be programmed, provided a program resistor, Rp, be connected between Ip (pin 8) and Ground (pin 9). The voltage at Ip (pin 8) is constant (≈1.3V). Thus, a current through Rp is $I_P \approx \frac{1.3V}{R_P}$, as shown in Figure 5. $\frac{I_O}{I_P}$ is 20 in the 15 to 50mA output current range.

4

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V T_A = 25°C. R_L = 130Ω, C_L = 30pF including probe capacity.

PARAMETER		TEST CONDITIONS	NE587			UNIT
			Min	Typ	Max	
$t_{D_{av.}}$	Propagation delay Figure 2	From data to output		135		ns
$t_{D_{av.}}$	Propagation delay Figure 3	From $\overline{LE}$ to output		135		ns
t_W	Latch enable pulse width Figure 4		30			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	20			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

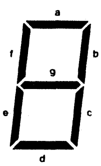
NOTE
$t_{D_{av.}} = ½ (t_{HL} + t_{LH})$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
–	H	•	X	X	X	X	STABLE							••	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	-
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	blank
••BI	X	X	X	X	X	X	H	H	H	H	H	H	H	L••	blank

NOTES
H = HIGH voltage level, output is "OFF"
L = LOW voltage level, output is "ON"
X = Don't care
• The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
•• $\overline{RBO}/\overline{BI}$ used as an input overrides all other input conditions.

SEGMENT IDENTIFICATION



NE587 PROGRAMMING

NE587 output current can be programmed by using a programming resistor, R_P, connected between rp (pin 8) and Gnd (pin 9). The voltage at rp (pin 8) is constant ($\approx$1.40V). A partial schematic of the voltage reference used in the NE587 is shown in figure 1.

Output current to program current ratio, I_O/I_P, is 20 in the 15mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

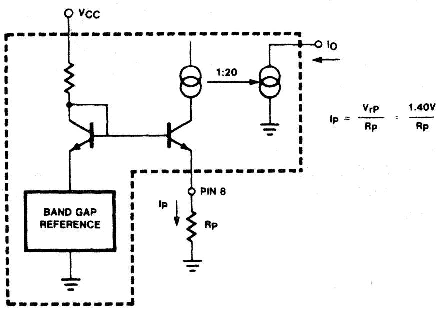


Figure 1

TIMING DIAGRAMS

PROPAGATION DELAY, DATA TO OUTPUT

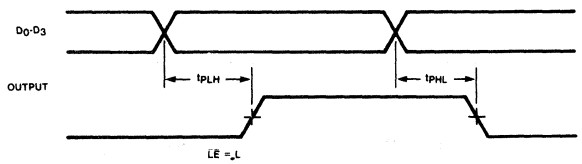


Figure 2

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

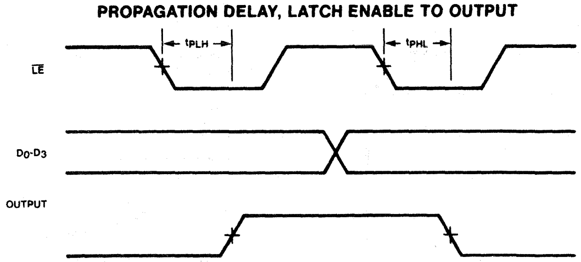


Figure 3

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDS are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to figure 6, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC},	Supply voltage to driver
V_S,	Supply voltage to display
I_{CC},	Quiescent supply current of driver
I_{SEG},	LED segment current
V_F,	LED segment forward voltage at I_{seg}
K_{DC},	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

TIMING DIAGRAMS (Cont'd)

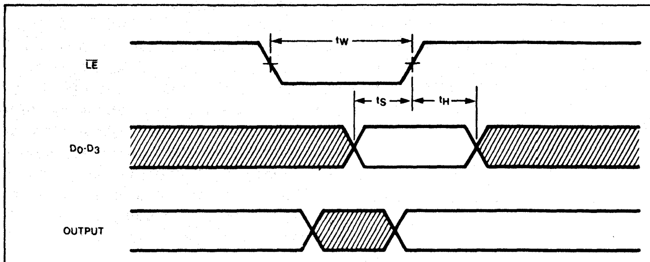


Figure 4

These voltages are all for single diode displays. Some early red displays had 2 series LEDS per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

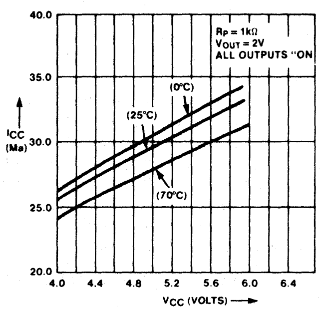
$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC}$ mW

Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$

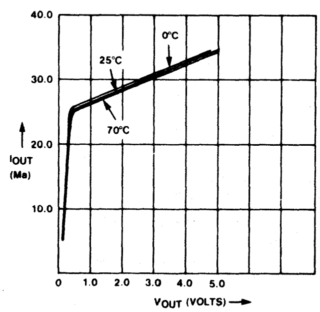
$P_{d\,max} = 5.25 \times 50 + 3.25 \times 7 \times 30$ mW
$= 945$ mW

TYPICAL PERFORMANCE CURVES

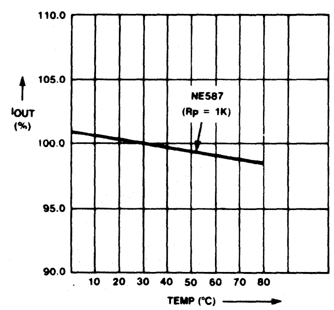
SUPPLY CURRENT VS SUPPLY VOLTAGE NE587



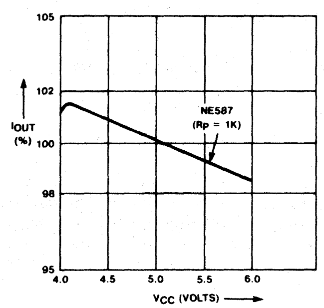
OUTPUT CURRENT VS OUTPUT VOLTAGE NE587 Rp = 1Kohms



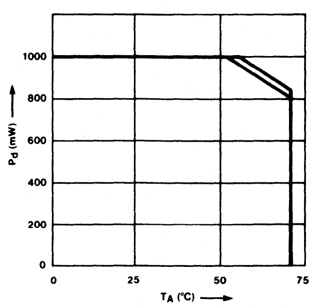
NORMALIZED OUTPUT CURRENT VS TEMPERATURE $V_{CC} = 5.0V$



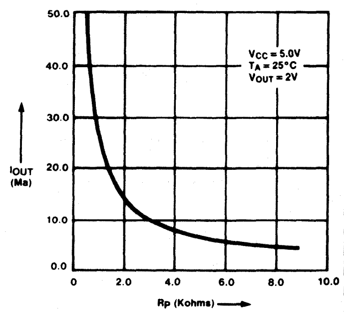
NORMALIZED OUTPUT CURRENT VS SUPPLY VOLTAGE $V_O = 2V$ $T_A = 25°C$



MAXIMUM POWER DISSIPATION VS TEMPERATURE

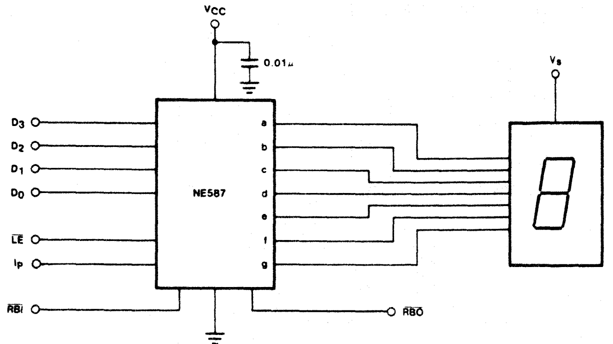


OUTPUT CURRENT VS PROGRAM RESISTOR



TYPICAL APPLICATIONS

DRIVING A SINGLE DIGIT



NOTE
Decoupling capacitor on V_{CC} should be 0.01 µF ceramic

Figure 6

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$P_{d\ av}$ = 5.0 × 30 + 3.00 × 5 × 25 mW
= 525 mW

Operating temperature range limitations can be deduced from the power dissipation graph. (See Typical Performance Characteristics).

However, a major portion of this power dissipation ($P_{d\ max}$) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{seg}} \simeq 10\Omega \text{ (½ W rating)}$$

assuming worst case I_{seg} of 30 mA

Hence now $P_{d\ max} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{seg}) \times 7 \times X\, I_{seg} \times K_{DC}$
= 5.25 × 50 + 1.25 × 7 × 30 mW
= 525 mW

and $P_{d\ av}$ = 5.0 × 30 + 1.25 × 5 × 25
= 306 mW

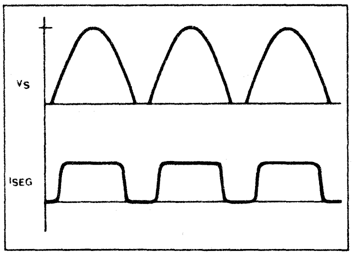
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_d,\ V_D \simeq 0.8V$$

Where n is the number of diodes used, power dissipation can be calculated in a similiar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 9. For example a darlington PNP or NPN emitter follower may be preferable. Figure 8 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
V_S = 4.9V pk.
V_F = 2.0V

The duty cycle is approximately 60%.

4

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT DISPLAY WITH BRIGHTNESS CONTROL AND LEADING EDGE RIPPLE BLANKING

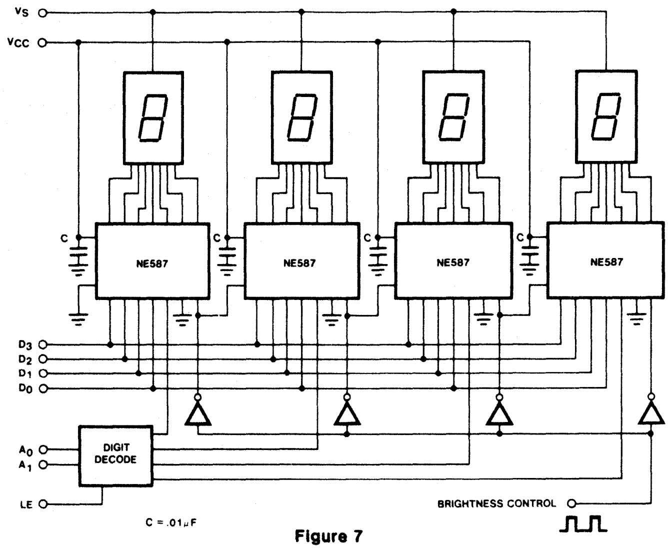


Figure 7

INTERFACING 8-DIGIT LED DISPLAY WITH µP BUS

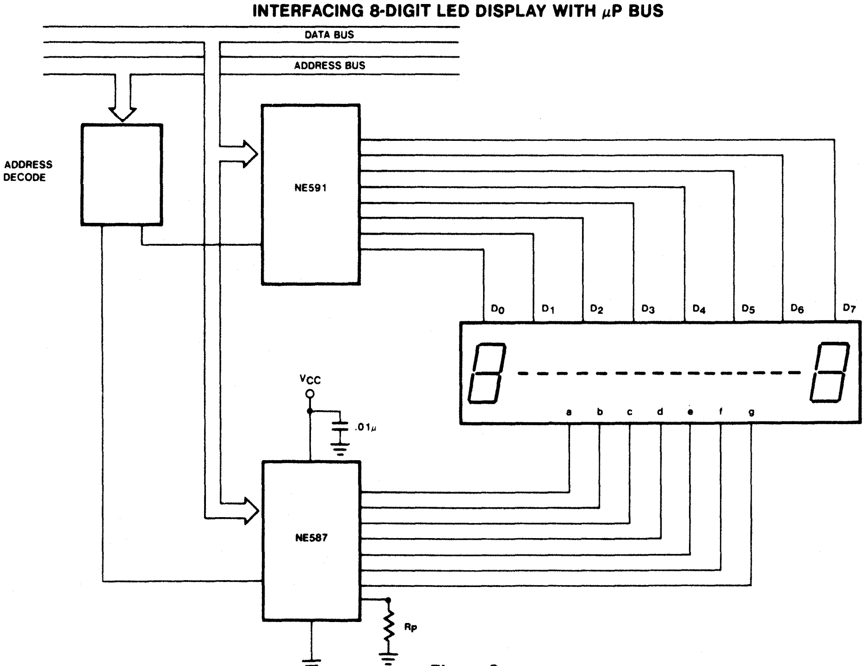


Figure 8

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT MULTIPLEXED LED DISPLAY

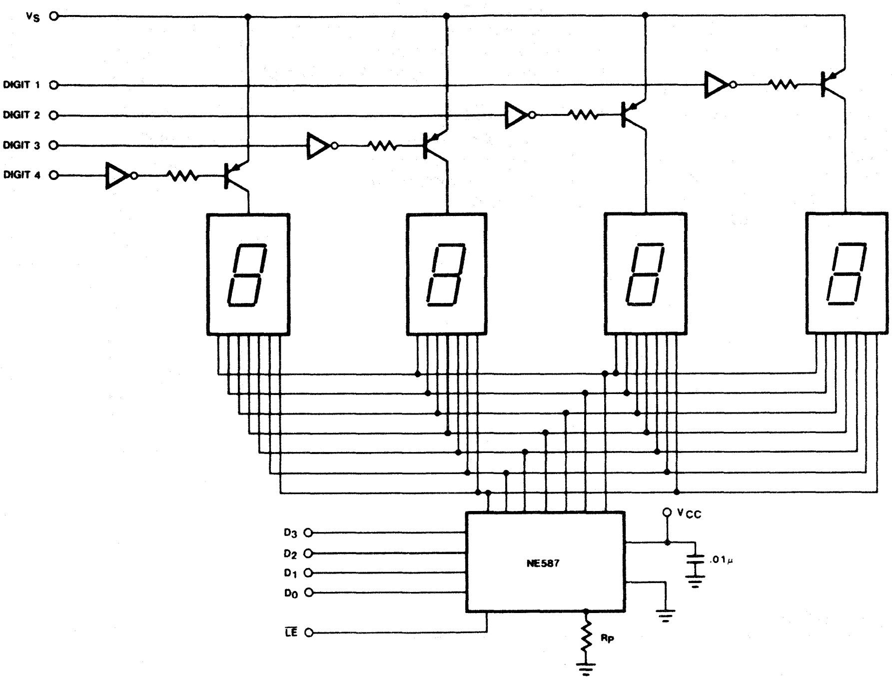


Figure 9

For additional information, refer to the Applications Section.

LVDT Signal Conditioner

SE/NE5521

DESCRIPTION

The SE/NE5521 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LVDT's) and Rotary Variable Differential Transformers (RVDT's). The chip includes a low distortion, amplitude stable sine wave oscillator with programmable frequency to drive the primary of the LVDT/RVDT, a synchronous demodulator to convert the LVDT/RVDT output amplitude and phase to position information, and an output amplifier to provide amplification and filtering of the demodulated signal.

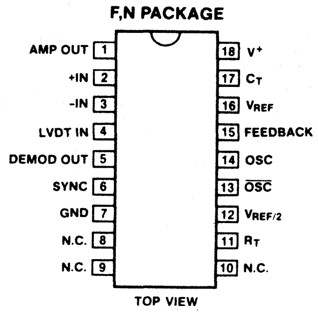
FEATURES

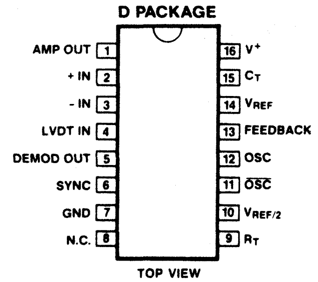
- **Low distortion**
- **Single supply 5V to 20V, or dual supply ±2.5V to ±10V**
- **Oscillator frequency 1kHz to 20kHz**
- **Capable of ratiometric operation**
- **Low power consumption (182mW typ)**

APPLICATIONS

- **LVDT signal conditioning**
- **RVDT signal conditioning**
- **LPDT signal conditioning**
- **Bridge circuits**

PIN CONFIGURATION

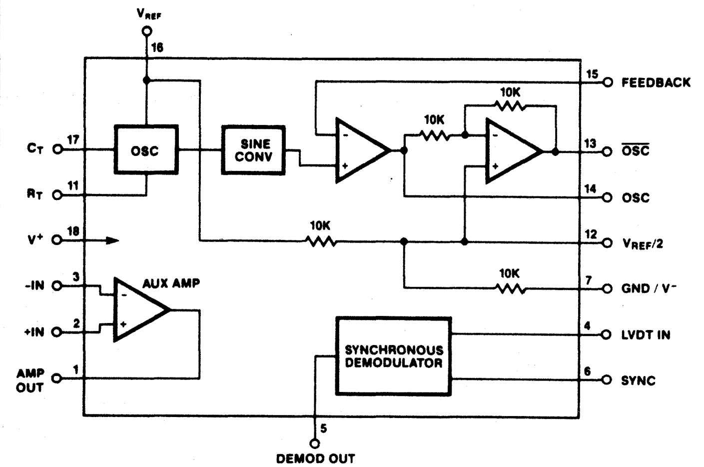




ORDER NUMBERS

NE5521N	SA5521N
NE5521F	SE5521F
NE5521D	

BLOCK DIAGRAM



Pin numbers are for F, N packages.

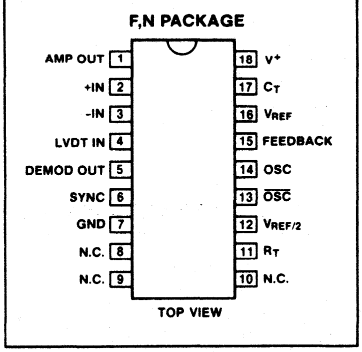
LVDT SIGNAL CONDITIONER

SE/NE5521

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+20	V
Split supply voltage	±10	V
Operating temperature range		
NE5521	0 TO +70	°C
SA5521	-40 TO +85	°C
SE5521	-55 TO +125	°C
Storage temperature range	-65 TO +150	°C
Power dissipation	840	mW

PIN CONFIGURATION



PIN DEFINITIONS

1	**Amp Out**	Auxiliary Amplifier Output.
2	**+IN**	Auxiliary Amplifier non-inverting input.
3	**-IN**	Auxiliary Amplifier inverting input.
4	**LVDT IN**	Input to Synchronous Demodulator from the LVDT/RVDT secondary.
5	**DEMOD OUT**	Pulsating DC output from the Synchronous Demodulator output. This voltage should be filtered before use.
6	**SYNC**	Synchronizing input for the Synchronous Demodulator. This input should be connected to the OSC or $\overline{\text{OSC}}$ output. Sync is referenced to $V_{REF}/2$.
7	**GND**	Device return. Should be connected to system ground or to the negative supply.
8	**NC**	No internal connection.
9	**NC**	No internal connection.
10	**NC**	No internal connection.
11	**R_T**	Oscillator frequency-determining resistor. A temperature stable 18K-ohm resistor should be connected between this pin and pin 7.
12	**$V_{REF}/2$**	A high impedance source of one half the potential applied to V_{REF} (pin 16). The LVDT/RVDT secondary return should be to this point. A bypass capacitor with low impedance at the oscillator frequency should also be connected between this pin and ground.
13	**$\overline{\text{OSC}}$**	Oscillator sinewave output that is 180° out of phase with the OSC signal at pin 14. The LVDT/RVDT primary is usually connected between OSC and $\overline{\text{OSC}}$ pins.
14	**OSC**	Oscillator sine wave output. The LVDT/RVDT primaries are usually connected between OSC and $\overline{\text{OSC}}$ pins.
15	**FEEDBACK**	Usually connected to the OSC (pin 14) output for unity gain. A resistor between this pin and OSC, and one between this pin and ground, can provide for a change in the oscillator output pin amplitudes.
16	**V_{REF}**	Reference voltage input for the oscillator and sine converter. This voltage MUST be stable and must never exceed V^+ supply voltage.
17	**C_T**	Oscillator frequency-determining capacitor. The capacitor connected between this pin and ground should be a temperature-stable type.
18	**V^+**	Positive supply connection.

ELECTRICAL CHARACTERISTICS $V+ = V_{REF} = 10V$, $T_A = 0$ to 70°C for NE5521, $T_A = -55$ to +125°C for SE5521, $T_A = -40$ to +85°C for SA5521, Frequency = 1kHz, unless otherwise noted.

PARAMETER	CONDITIONS	NE5521			SA/SE5521			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply current			12.9	20		12.9	18	mA
Reference current			5.3	8		5.3	8	mA
Reference voltage range		5		V^+	5		V^+	V
Power dissipation			182	280		182	260	mW
Oscillator Section								
Oscillator Output	$R_L = 10K$		$\frac{V_{REF}}{8.8}$			$\frac{V_{REF}}{8.8}$		V_{rms}
Sine wave distortion	No Load		1.5			1.5		%
Initial amplitude error	$T_A = 25°C$		0.4	±3		0.4	±3	%
Tempco of amplitude			0.005	0.01		0.005	0.01	% / °C
Init. accuracy of oscillator freq.	$T_A = 25°C$		±0.9	±5		±0.9	±5	%
Temperature coeff. of frequency[1]			0.05			0.05		% / °C
Voltage coeff. of frequency			2.5			3.3		% / $V(V_{REF})$
Min OSC to ($\overline{OSC}$) Load[2]		300	170		300	170		Ω
Demodulator Section								
Linearity error	5 V_{p-p} input		±0.05	±0.1		±0.05	±0.1	% FS
Maximum demodulator input			$\frac{V_{REF}}{2}$			$\frac{V_{REF}}{2}$		V_{p-p}
Demodulator offset voltage			±1.4	±5		±1.4	±5	mV
Demodulator offset voltage drift			5	25		5	25	μV / °C
Demodulator input current		-600	-234		-500	-234		nA
$V_R/2$ accuracy			±0.1	±1		±0.1	±1	%
Auxiliary Output Amplifier								
Input offset voltage			±0.5	±5		±0.5	±5	mV
Input offset drift			±2	±25		±2	±25	μV / °C
Input bias current		-600	-210		-500	-210		nA
Input offset current			9	50		9	50	nA
Gain		100	385		100	385		V/mV
Slew rate			1.3			1.3		V/μSec
Unity gain bandwidth product	$A_V = 1$		1.6			1.6		MHz
Output voltage swing	$R_L = 10K$	7	8.2		7	8.2		V
Output short circuit current to ground or to V_{cc}	$T_A = 25°C$		42	100		42	100	mA

NOTES
1. This is temperature coefficient of frequency for the device only. It is assumed that C_T and R_T are fixed in value and C_T leakage is fixed over the operating temperature range.
2. Minimum load impedance for which distortion is guaranteed to be less than 5%.

LVDT SIGNAL CONDITIONER SE/NE5521

EXPLANATION OF TERMS

Oscillator Output	rms value of the AC voltage available at the oscillator output pin. This output is referenced to $V_{REF}/2$ and is a function of V_{REF}.
Sine Wave Distortion	The Total Harmonic Distortion (THD) of the oscillator output with no load. This is not a critical specification in LVDT/RVDT system. This figure could be 15% or more without affecting system performance.
Initial Amplitude Error	A measure of the interchangeability of SE/NE5521 parts, NOT a characteristic of any one part. It is the degree to which the oscillator output of a number of SE/NE5521 samples will vary from the median of that sample.
Initial Accuracy of Oscillator Frequency	Another measure of the interchangeability of individual SE/NE5521 parts. This is the degree to which the oscillator frequency of a number of SE/NE5521 samples will vary from the median of that sample with a given timing capacitor.
Tempco of Oscillator Amplitude	A measure of how the oscillator amplitude varies with ambient temperature as that temperature deviates from a 25°C ambient.
Tempco of Oscillator Frequency	A measure of how the oscillator frequency varies with ambient temperature as that temperature deviates from a 25°C ambient.
Voltage Coeffecient of Oscillator Frequency	The degree to which the oscillator frequency will vary as the reference voltage (V_{REF}) deviates from +10 volts.
Linearity Error	The degree to which the DC output of the demodulator/amplifier combination matches a change in the AC signal at the demodulator input. It is measured as the worst case nonlinearity from a straight line drawn between positive and negative full scale end points.
Maximum Demodulator Input	The maximum signal that can be applied to the demodulator input without exceeding the specified linearity error.

4

APPLICATION INFORMATION

$$\text{OSC frequency} = \frac{V_{REF} - 1.3V}{V_{REF}(R_T + 1.5K)C_T}$$

Section 5
Communication

INDEX

SECTION 5 – COMMUNICATION

Double Balanced Mixer and Oscillator

SA/NE602

DESCRIPTION

The SA/NE602 is a monolithic Double Balanced Mixer with on-board oscillator and voltage regulator. The oscillator can be used as a buffer for external injection. The design is optimized for frequency conversion applications up to 200MHz and has excellent noise and 3rd order intermodulation performance. The SA/NE602 is available in a 8 lead dual in line plastic package and 8 lead SO (Surface mounted miniature package).

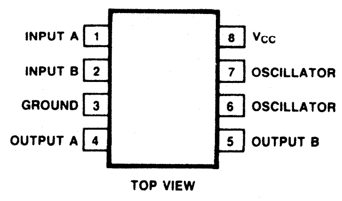
FEATURES

- **Low current consumption: 2.4mA typical**
- **High input and oscillator frequency operation up to 200MHz**
- **High third order intercept point: −15 dBm referred to matched input**
- **Excellent noise figure: 5.0dB typical at 45 MHz**
- **Low external count; suitable for crystal/ceramic filters**

APPLICATIONS

- **HF and VHF frequency conversion**
- **Cellular radio mixer/oscillator**
- **Communication receivers**
- **Instrumentation frequency converters**
- **VHF walkie talkie**

PIN CONFIGURATION



ORDER PART NUMBERS

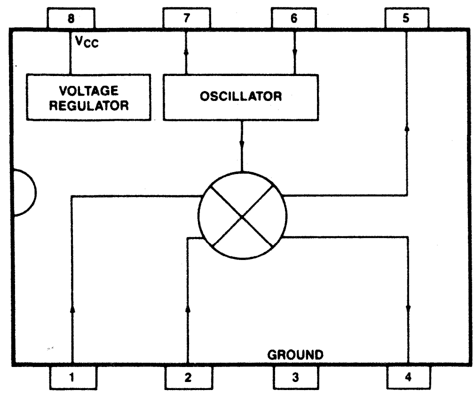
NE602N SA602N
NE602D SA602D

5

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	9	V
Storage temperature	−65 to +150	°C
Operating temperature NE602 SA602	 0 to +70 −40 to +85	 °C °C

BLOCK DIAGRAM



Double Balanced Mixer and Oscillator SA/NE602

DC ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 6V$.

SYMBOL AND PARAMETER	SA/NE602 Min	Typ	Max	UNIT
Power supply voltage range	4.5	—	8.0	V
D.C. current drain	—	2.4	2.7	mA
Input signal frequency	—	—	200	MHz
Oscillator frequency	—	—	200	MHz
Noise figure @ 45MHz	—	5.0	6	dB
Third order intercept point	—	−15	−17	dBm
Mixer input resistance	1.5	—	—	kΩ
Mixer input capacitance	—	3	3.5	pF
Mixer output resistance[1]	—	2 x 1.5	—	kΩ

NOTE:
1. Each output pin is internally connected to V_{CC} through a 1.5 (nominal) kΩ resistor.

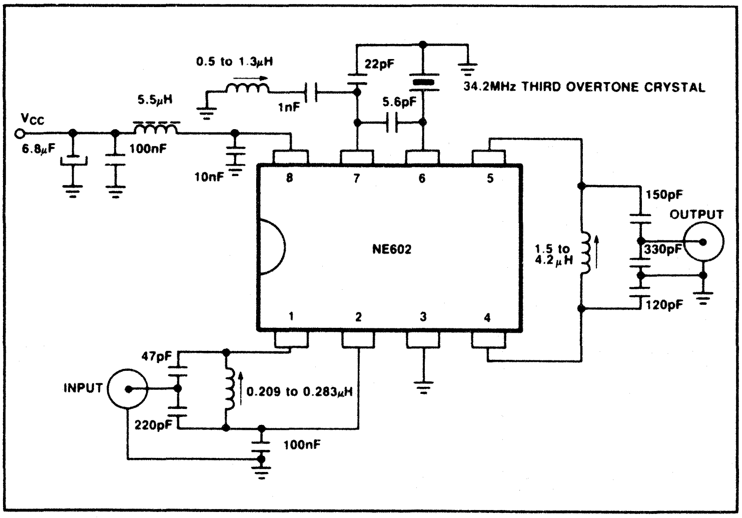
CIRCUIT DESCRIPTION

The NE602 utilizes an active double balanced mixer. The RF input port (pins 1 and 2) can be used in either a symmetrical or an asymmetrical configuration. The RF input port has a resistance of 1.5KΩ shunted by 3.0pF. In order to be used as an asymmetrical configuration, one of the two input pins (1 or 2) must be bypassed to ground with a capacitor. The RF input port does not need any external bias and should not be DC grounded. An external DC path between pins 1 and 2 is allowed.

The local oscillator is an emmitter-follower circuit and is capable of many types of oscillator configurations. Pin 6 (oscillator base) and pin 7 (oscillator emitter) do not need any external bias circuitry, but only pin 6 may have a DC path to V_{CC}. Pin 6 can be used for external oscillator or for frequency synthesizer injection.

The NE602 output pins can be used in a single-ended or push-pull configuration. There are internal 1.5KΩ resistors connected to V_{CC} for each output pin (4 and 5); therefore no external bias is needed. Pins 4 and/or 5 may have a DC path to V_{CC}.

TYPICAL APPLICATION



Low Power FM I.F. System

SA/NE604

DESCRIPTION

The SA/NE604 is a monolithic low power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The SA/NE604 is available in a 16 lead dual-in-line plastic package and 16 lead SO (surface mounted miniature package).

FEATURES

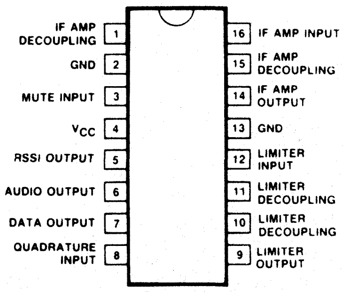
- **Low power consumption: 2.3mA typical**
- **Logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Separate data output**
- **Audio output with muting**
- **Low external count; suitable for crystal/ceramic filters**
- **Excellent sensitivity: 1.5μV across input pins (0.27 μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz**

APPLICATIONS

- **Cellular Radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 10.7MHz**
- **RF level meter**
- **Spectrum analyzer**

PIN CONFIGURATION

N, D PACKAGE



TOP VIEW

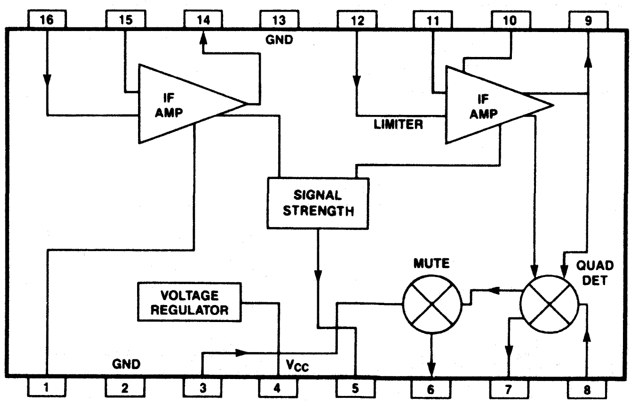
ORDER NUMBERS

NE604N, NE604D
SA604N, SA604D

ABSOLUTE MAXIMUM RATINGS

SYMBOL AND PARAMETER	RATING	UNIT
Maximum operating voltage	9	V
Storage temperature	-65 to +150	°C
Operating temperature		
NE604	0 to +70	°C
SA604	-40 to +85	°C

BLOCK DIAGRAM



Low Power FM I.F. System SA/NE604

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +6$ volts, unless otherwise stated.

SYMBOL AND PARAMETER	SA/NE604 Min	Typ	Max	UNITS
Power supply voltage range	4.5	-	8.0	V
D.C. current drain	-	2.3	2.7	mA
I.F. frequency	-	-	10.7	MHz
RSSI range	TBD	90	-	dB
RSSI accuracy	-	±1.5	-	dB
I.F. input impedance	1.5	-	-	kΩ
I.F. output impedance	1.0	-	-	kΩ
Limiter input impedance	1.5	-	-	kΩ
Quadrature detector data output impedance	50	-	-	kΩ
Muted audio out impedance	-	50	-	kΩ
Mute - switch input threshold (on)	1.7	-	-	V
(off)	-	-	1.0	V

CIRCUIT DESCRIPTION

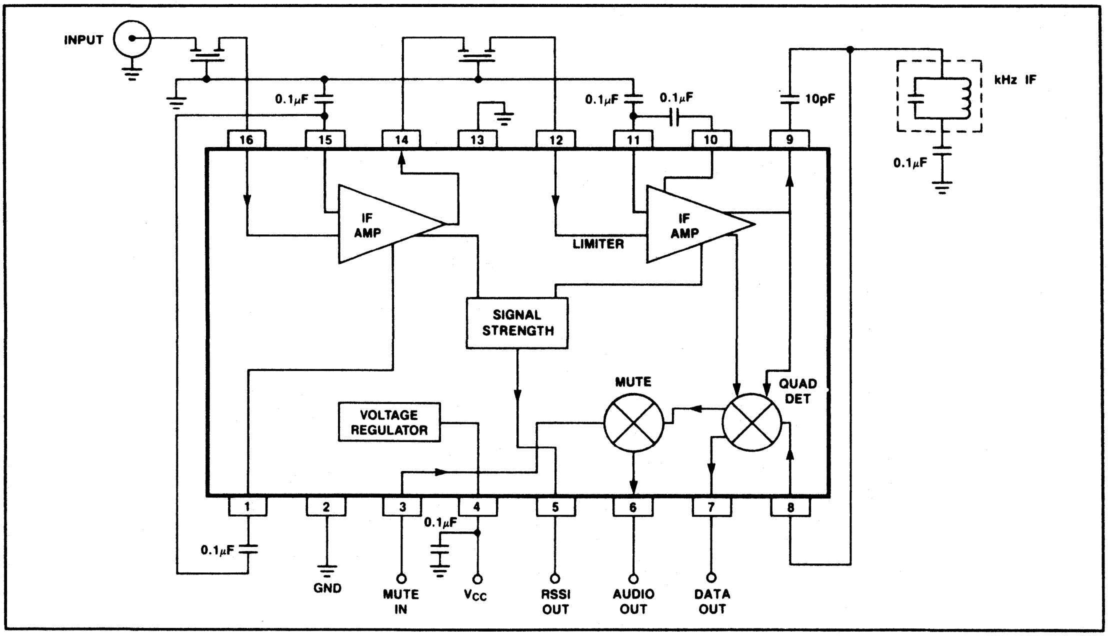
The SA/NE604's IF amplifier has a gain of 30dB, bandwidth of 15MHz, with an input impedance of 1.5KΩ and an output impedance of 1.0KΩ. The limiter has a gain of 60dB, bandwidth of 15MHz, and an input impedance of 1.5KΩ. An interstage filter between the IF Amplifier and Limiter is recommended to reduce wideband noise. The quadrature detector input (pin 8) impedance is 40KΩ.

The data (unmuted output) and audio (muted output) both have 50KΩ output impedance and their detected signals are 180 degrees out of phase with each other. The mute input (pin 3) has a very high impedance and is compatible with three and five volt CMOS and TTL levels. Little or no DC level shift occurs after muting when the quadrature detector is adjusted to the IF center frequency. Muting will attenuate the audio signal by more than 60dB and no voltage spikes will be generated by muting.

The logarithmic signal strength indicator is a current source output with maximum source current of 50 microamps. The signal strength indicator's transfer function is approximately 10 microamp per 20dB and is independent of IF frequency. The interstage filter must have a 6dB insertion loss to optimize slope linearity.

Pins 1, 16, 15, 14, 12, 11, 10, 9, and 8 do not need external bias and should not have a DC path.

TYPICAL APPLICATION



Low Voltage Dolby B / C Type IC

NE670

DESCRIPTION

The NE670 is a monolithic IC intended for use in low voltage Dolby* B & C type noise reduction applications. This IC design features both record and play-back mode with all internal electronic switching.

FEATURES

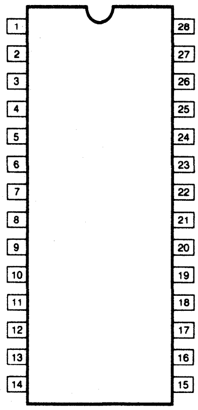
- **B and C type noise reduction**
- **Low voltage operation 1.8–8V**
- **Playback and record modes**
- **0dB (Dolby level) = 100mV**
- **Record input sensitivity 50mV**
- **Playback sensitivity 20mV**
- **All electronic switching**

APPLICATION

- **Portable tape recorders/players**

PIN CONFIGURATION

D PACKAGE



TOP VIEW
Order Numbers
NE670D

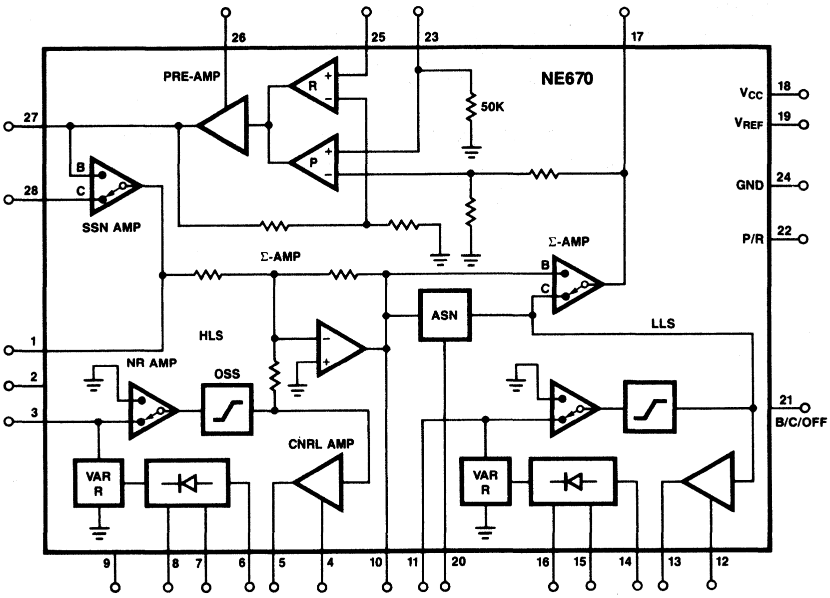
Pin Function

1. Test point
2. Internal switch
3. High-level stage side chain input
4. High-level stage high pass
5. High-level stage D-amp output
6. High-level stage rectifier input
7. High-level stage attack
8. High-level stage decay
9. Internal switch
10. High-level stage output
11. Low-level side chain input
12. Low-level stage high pass
13. Low-level stage D-amp output
14. Low-level stage rectifier input
15. Low-level stage attack
16. Low-level stage decay
17. Record output
18. V_{CC}
19. V_{REF}
20. Anti-saturation network capacitor
21. Mode switch
22. Playback record switch
23. Play input
24. Ground
25. Record input
26. Compensation capacitor
27. Line output
28. Spectral skewing network

*Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and application information must be obtained.
Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Francisco, California.

Low Voltage Dolby B/C Type IC | NE670

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL & PARAMETER		RATING	UNIT
V_{CC}	Supply Voltage	8	V
	Temperature Range		
T_A	Operating	0 to +70	°C
T_{STG}	Storage	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

Standard Conditions: $V_{CC} = 3V$, $T_A = 25°C$.
All levels referenced to 0dB = 100mV at test point (TP).

SPECIFICATION	B/C	NR	MODE	CONDITIONS	LIMITS Min	Typ	Max	UNIT
Voltage range V_{CC}		Off	R		1.8	3	8	V
Min functional V_{CC}		Off	R	THD 1%		1.5		V
Distortion THD; 2nd and 3rd Harmonics	B	Off	R	0dB, f = 1kHz		0.02		%
	B	On	R			0.05	0.1	%
	C	On	R			0.1		%
Signal-to-Noise Ratio	B	Off	R	CCIR (DOLBY)		78		dB
		On	R	Rs = 10Kohms		74		dB
	C	On	R			66		dB
Supply current, I_{CC}	C	Off	R	0dB, f = 1kHz		7		mA
		On	R			9		mA
Signal handling	C	On	R	1% THD, $V_{CC} = 1.8V$	12			dB
	C	On	R	$V_{CC} = 3V$		14		dB
Input resistance				Pin 23	35	50	65	K
Frequency response (Referenced to test point)	B	On	R	f = 10kHz,OdB	−1.6	0.4	2.4	dB
	B	On	R	1kHz, −20dB	−17.8	−15.8	−13.8	dB
	B	On	R	5kHz, −30dB	−23.8	−21.8	−19.8	dB
	B	On	R	5kHz, −40dB	−31.7	−29.7	−27.7	dB
	C	On	R	10kHz, 0dB	−5.5	−3.5	−1.5	dB
	C	On	R	1kHz, −20dB	−16.1	−14.1	−12.1	dB
	C	On	R	5kHz, −40dB	−28.5	−26.5	−24.5	dB
	C	On	R	200Hz, −40B	−33.9	−31.9	−29.9	dB
Switching thresholds	B	Off			0	GND	$0.1V_{CC}$	V
						Open		V
	C				$0.95V_{CC}$	V_{CC}	V_{CC}	V
			P		0	GND	0.2	V
			R		$0.7V_{CC}$	V_{CC}	V_{CC}	V
Pre-Amp gain	B	Off	R			6		dB
			P			14		dB

NOTE:
R = record mode
P = play mode

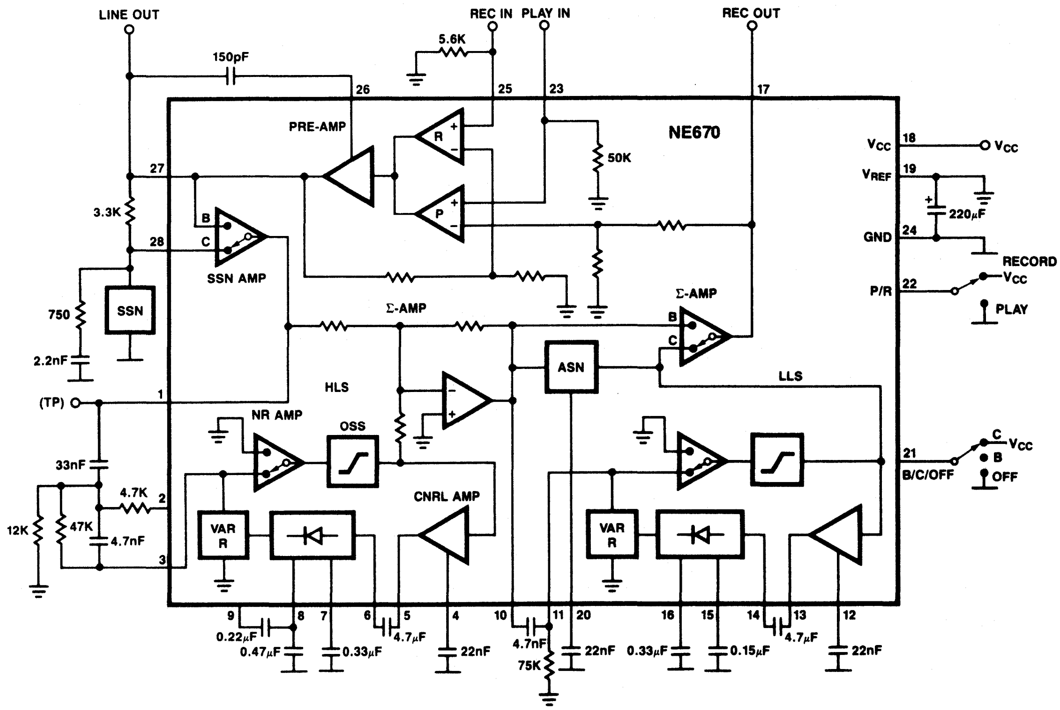


Figure 1. Test Circuit

Section 6
Amplifiers

INDEX

Wideband High Frequency Amplifier

NE5205

DESCRIPTION

The NE5205 is a High Frequency Amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the −3dB bandwidth is greater than 600MHz. This performance makes the amplifier ideal for cable TV applications. The NE5205 operates with a single supply of 6 volts, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75 ohm system and 6dB in a 50 ohm system.

Until now, most RF or high frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE5205 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75 ohm input and output impedances. The Standing Wave Ratios in 50 and 75 ohm systems do not exceed 1.5 on either the input or output over the entire DC to 600MHz operating range.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects. A TO-46 metal can is also available that has a case connection for RF grounding which increases the −3dB frequency to 650MHz. The metal can is hermetically sealed, and can operate over the full −55 to +125°C range.

No external components are needed other than AC coupling capacitors because the NE5205 is internally compensated and matched to 50 and 75 ohms. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75 ohm cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50 ohm test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50 ohms include mobile radio, CB radio and data/video transmission in fiber optics, as well as broadband LAN's and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE5205's in series as required, without any degradation in amplifier stability.

FEATURES:

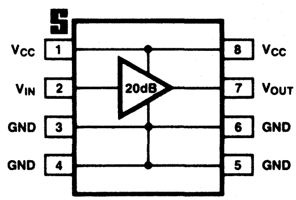
- **650MHz bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)**
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface-Mount package available**
- **Excellent performance in cable TV 75Ω systems**

APPLICATIONS

- **75Ω cable TV decoder boxes**
- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broadband LAN's**
- **Fiber optics**
- **Modems**
- **Mobile radio**
- **CB radio**
- **Telecommunications**

PIN CONFIGURATION

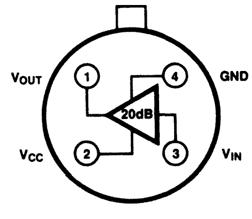
D PACKAGE



TOP VIEW
Order Number
NE5205D

NOTE: Signetics ■ designates Pin 1.

EC PACKAGE



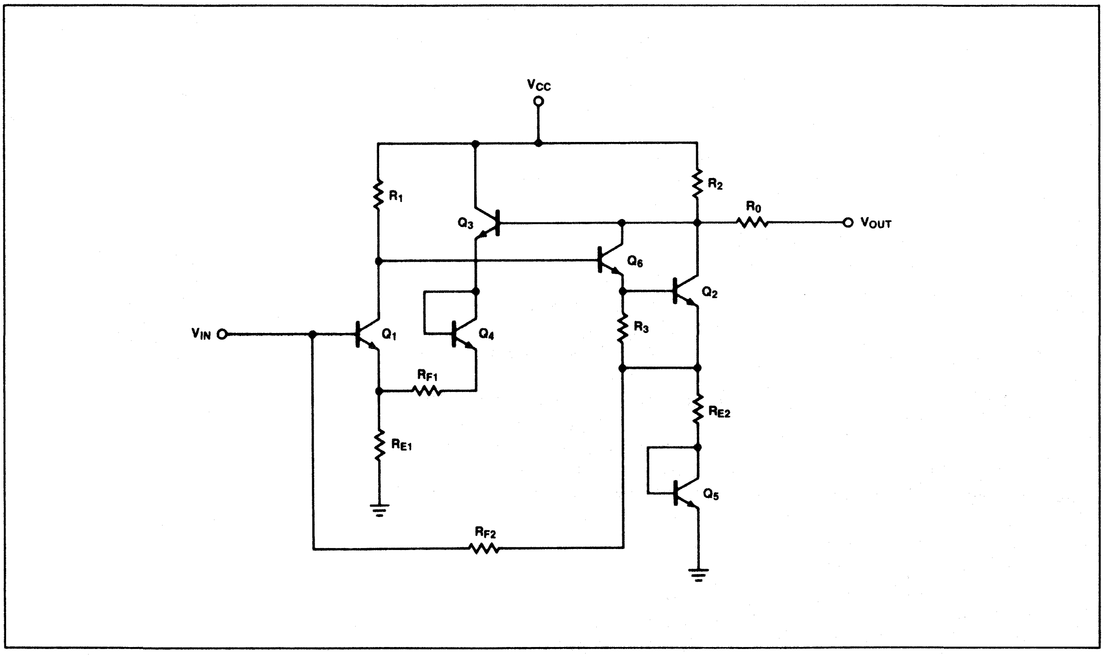
TOP VIEW
Order Number
NE5205EC

NOTE: Tab denotes Pin 1.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Supply Voltage	9	V
AC Input Voltage	5	V-PP
Operating Temperature		
SO package air-mount	−55 to +85	°C
TO package air-mount	−55 to +125	°C
(Derate SO package above 6V)		

EQUIVALENT SCHEMATIC



Wideband High Frequency Amplifier NE5205

DC ELECTRICAL CHARACTERISTICS at $V_{CC} = 6V$, $Z_S = Z_L = Z_0 = 50\Omega$ and $T_A = 25\ °C$, in SO package unless otherwise specified.

PARAMETER	TEST CONDITIONS	Min	Typ	Max	UNIT
Operating supply voltage range		5		8	V
Supply current		20	24	30	mA
Insertion gain – S21	f = 100MHz	17	19	21	dB
Input return loss – S11	f = 100MHz SO pkg		25		dB
	DC – 550MHz	12			dB
Input return loss – S11	f = 100MHz TO pkg		23		dB
	DC – 600MHz	10			dB
Output return loss – S22	f = 100MHz SO pkg		27		dB
	DC – 550MHz	12			dB
Output return loss – S22	f = 100MHz TO pkg		26		dB
	DC – 600MHz	10			dB
Isolation – S12 (SO, TO)	f = 100MHz		– 25		dB
	DC – 550MHz	– 18			dB
Bandwidth-SO	± 0.5dB		450		MHz
Bandwidth-SO	– 3dB	550	600		MHz
Bandwidth-TO	– 3dB	600	650		MHz
Noise figure (75Ω)	f = 100MHz		4.8		dB
Noise figure (50Ω)	f = 100MHz		6.0		dB
Saturated output power	f = 100MHz		+ 7.0		dBm
1dB gain compression	f = 100MHz		+ 4.0		dBm
Third-order intermodulation intercept (output)	f-100MHz		+ 17		dBm
Second-order intermodulation intercept (output)	f = 100MHz		+ 24		dBm

6

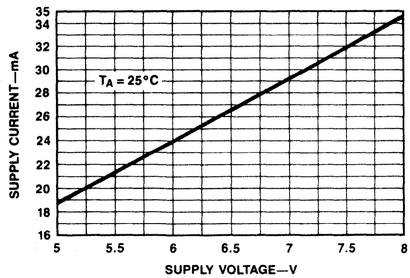


Figure 1. Supply Current vs Supply Voltage

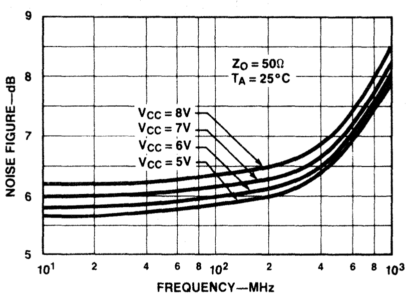


Figure 2. Noise Figure vs. Frequency

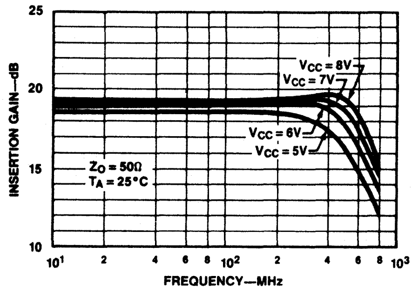


Figure 3. Insertion Gain vs Frequency (S_{21})

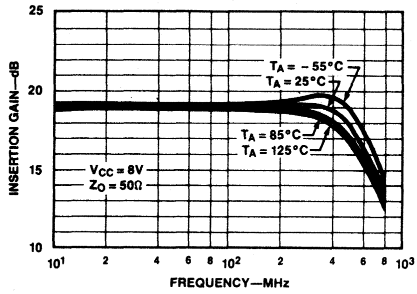


Figure 4. Insertion Gain vs Frequency (S_{21})

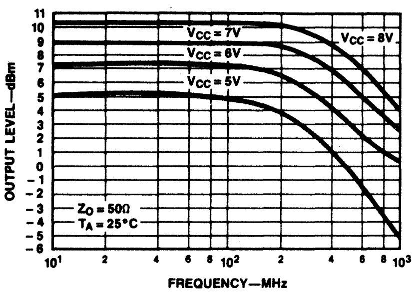


Figure 5. Saturated Output Power vs Frequency

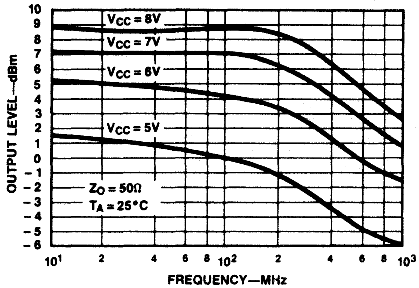


Figure 6. 1dB Gain Compression vs Frequency

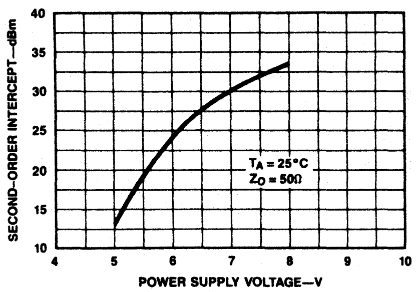


Figure 7. Second-Order Output Intercept vs Supply Voltage

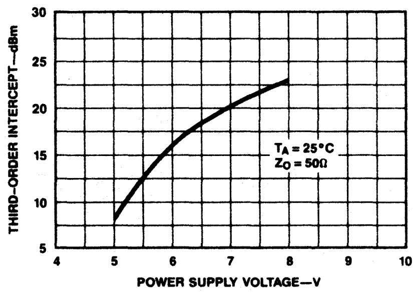


Figure 8. Third-Order Intercept vs Supply Voltage

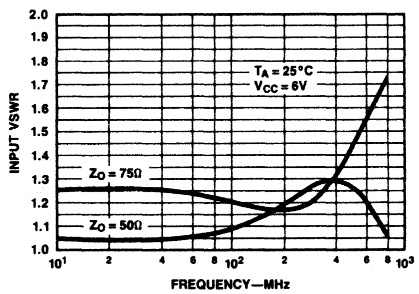


Figure 9. Input VSWR vs Frequency

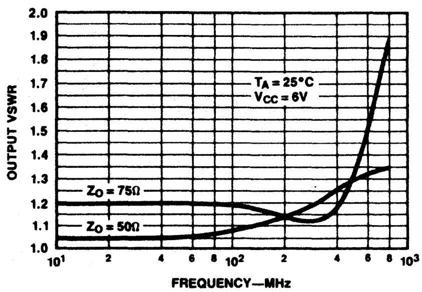


Figure 10. Output VSWR vs Frequency

6

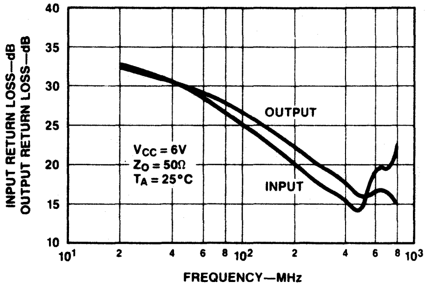


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

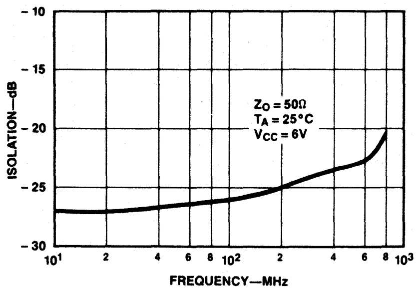


Figure 12. Isolation vs Frequency (S_{12})

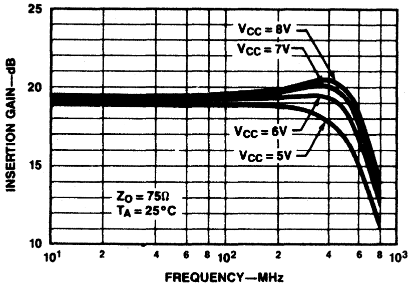


Figure 13. Insertion Gain vs Frequency (S_{21})

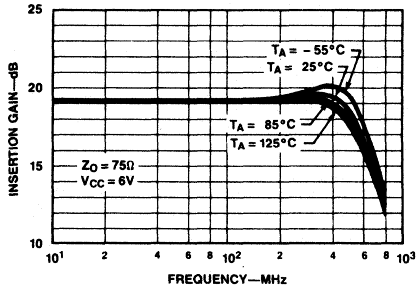


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wideband gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \qquad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure for 50 and 75 ohm systems is given by the following equation:

$$NF = 10 \text{ Log} \left\{ 1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}} \right]}{R_0} \right\} dB \qquad (2)$$

where $I_{C1} = 5.5mA$, $R_{E1} = 12\Omega$, $r_b = 130\Omega$, $KT/q = 26mV$ at 25°C and $R_0 = 50$ for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})R_{E1} \qquad (3)$$

where $R_{E1} = 12\Omega$, $V_{BE} = 0.8V$, $I_{C1} = 5mA$ and $I_{C3} = 7mA$ (currents rated at $V_{CC} = 6V$).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of $R_{F1} = 140$ ohms is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R_2, \qquad (4)$$

where $V_{CC} = 6V$, $R_2 = 225\Omega$, $I_{C2} = 7mA$ and $I_{C6} = 5mA$.

From here it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package. Signetics does not recommend operation at die temperatures above 110°C in the SO package. With this in mind, the following equation can be used to estimate the die temperature:

$$T_j = T_A + (P_d \times \theta_{jA})$$

where T_A = Ambient Temperature, T_j = Die Temperature, P_d = Power Dissipation = $I_{CC} \times V_{CC}$, θ_{jA} = Package Thermal Resistance, and θ_{jA} = 270°C/watt for SO-8, θ_{jA} = 100°C/watt for TO-46.

At the nominal supply voltage of 6 volts, the typical supply current is 25mA (30mA Max). For operation at supply voltages other than 6 volts, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either tempera-

6

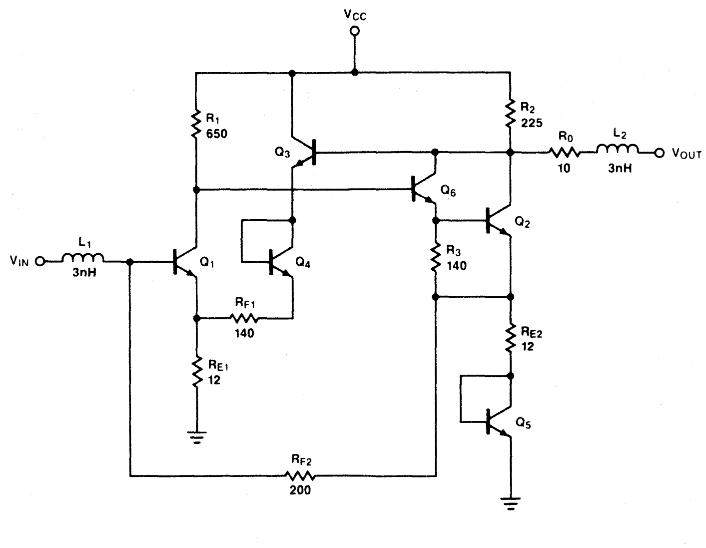


Figure 15. Schematic Diagram

ture extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the SO and TO-46 package body against the PC board plane. Operation at higher temperatures is possible but may result in lower MTBF (Mean Time Between Failures). This lower MTBF should be considered before operating beyond 110°C die temperature because of the overall reliability degradation.

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). In addition, if the TO-46 package is used, the case should be soldered to the ground plane. The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at $V_{CC} = 6V$, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

Both of the evaluation boards that will be discussed next do not have input an output capacitors because it is assumed the user will use AC coupled test systems. Chip or foil capacitors can easily be inserted between the part and connector if the board trace is removed.

50 OHM EVALUATION BOARD

The evaluation board layout shown in Figure 17 produces excellent results. The board is to scale and is for the SO package but can be

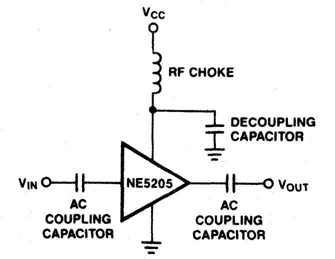
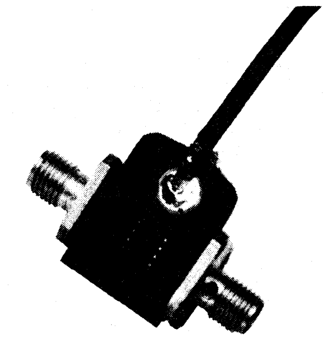


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling



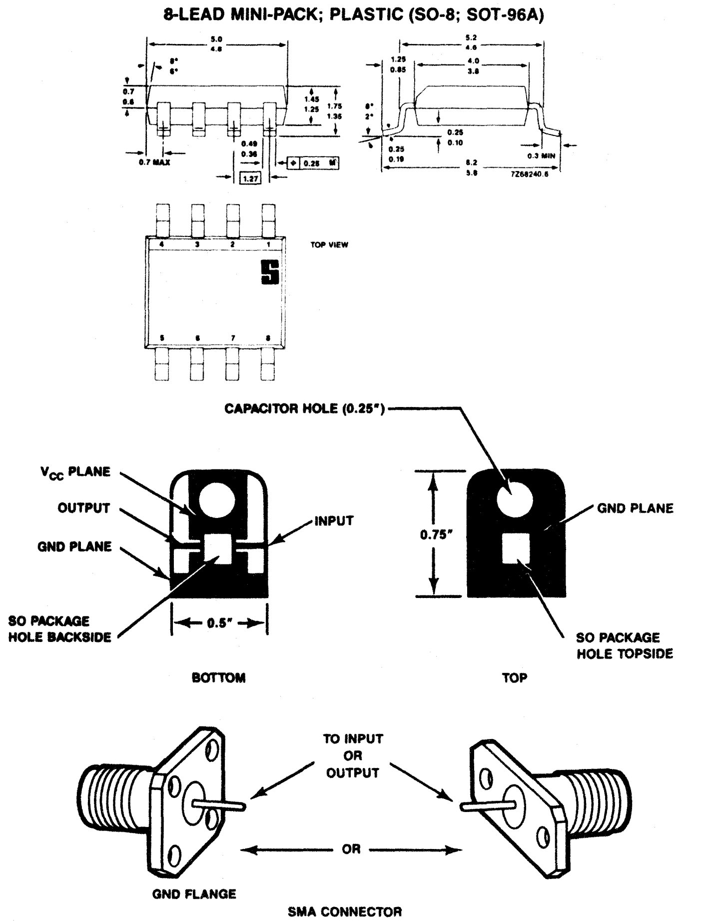


Figure 17. BC Board Layout for NE5205 Evaluation

used for the TO-46 package as well. Both top and bottom are copper clad and the ground planes are bonded together through 50 ohm SMA cable connectors. These are solder mounted on the sides of the board so that the signal traces line up straight to the connector signal pins.

Solid copper tubing is soldered through the flange holes between the two connectors for increased strength and grounding characteristics. Two or four hole flanges can be used. A flat round decoupling capacitor is placed in the board's round hole and soldered between the bottom V_{CC} plane and the top side ground. The capacitor is as thin or thinner than the PC board thickness and has insulation around its side to isolate V_{CC} and ground. The square hole is for the SO package which is put in upside down through the bottom of the board so that the leads are kept in position for soldering. Both holes are just slightly larger than the capacitor and IC to provide for a tight fit.

This board should be tested in a system with 50 ohm input and output impedance for correct operation.

75 OHM EVALUATION BOARD

Another evaluation board is shown in Figure 18. This system uses the same PC board as presented in Figure 17, but makes use of 75 ohm female N-type connectors. The board is mounted in a nickel plated box* that is used to support the N-type connectors. This is an excellent way to test the part for cable TV applications. Again, the board should be tested in a system with 75 ohm input and output impedance for correct operation.

*The box and connectors are available as a "MODPACK SYSTEM" from the ANZAC division of ADAMS-RUSSELL CO., INC., 80 Cambridge Street, Burlington, MA 01803.

SCATTERING PARAMETERS

The primary specifications for the NE5205 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 19.

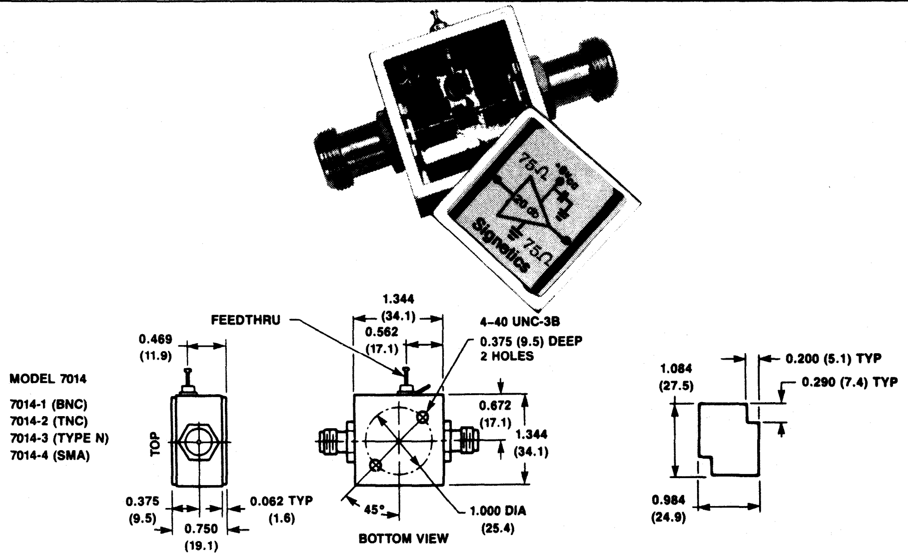


Figure 18. 75-Ohm N-Type Connector System

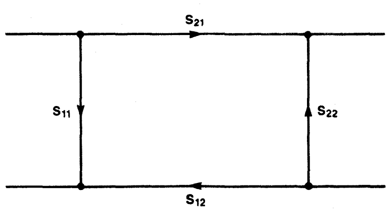


Figure 19a. Two-Port Network Defined

Wideband High Frequency Amplifier NE5205

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

Figure 19b

Actual S-parameter measurements using an H.P. network analyzer (model 8505A) and an H.P. S-parameter tester (models 8503A/B) are shown in Figure 20. These were obtained with the device mounted in a PC board as described in Figures 17 and 18.

For 50 ohm system measurements, SMA connectors were used. The 75 ohm data was obtained using N-connectors.

Values for the figures below are measured and specified in the data sheet to ease adap-

50Ω System

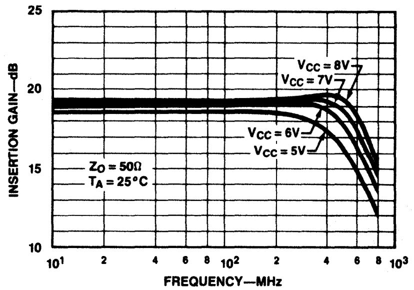


Figure A. Insertion Gain vs Frequency (S_{21})

75Ω System

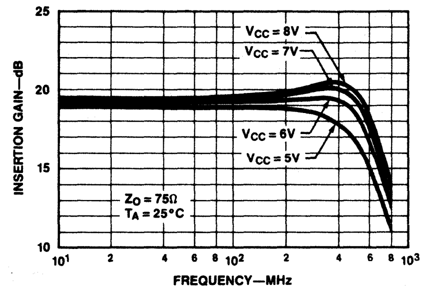


Figure B. Insertion Gain vs Frequency (S_{21})

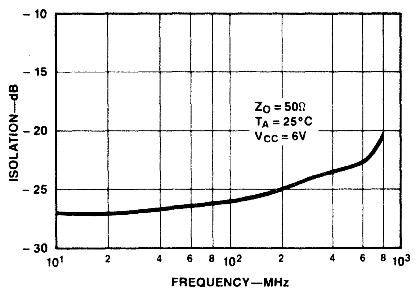


Figure C. Isolation vs Frequency (S_{12})

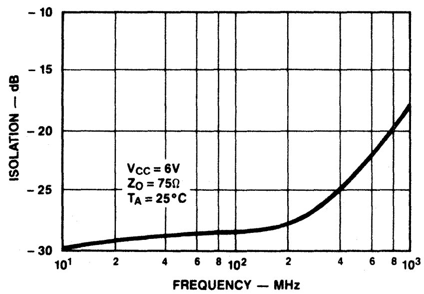


Figure D. S_{12} Isolation vs Frequency

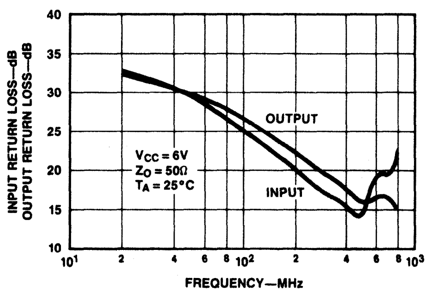


Figure E. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

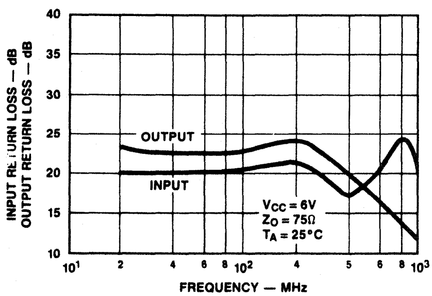


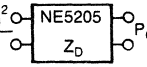
Figure F. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 20

tation and comparison of the NE5205 to other high frequency amplifiers. The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE5205

$$P_{IN} = \frac{V_{IN}^2}{Z_D} \qquad P_{OUT} = \frac{V_{OUT}^2}{Z_D}$$



$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I = Insertion Power Gain

V_I = Insertion Voltage Gain

Measured value for the NE5205 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$$

$$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$$

$$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 21. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = S_{11}dB
$S_{11}\text{dB} = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS = S_{22}dB
$S_{22}\text{dB} = 20 \text{ Log } |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leq 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leq 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 22, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope respectively.

The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$$IP_2 = P_{OUT} + IMR_2$$

$$IP_3 = P_{OUT} + IMR_3/2$$

6

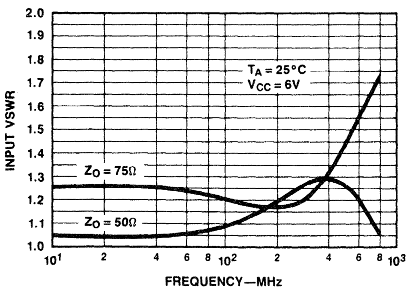


Figure A. Input VSWR vs Frequency

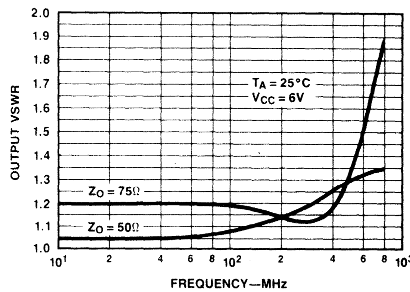


Figure B. Output VSWR vs Frequency

Figure 21. Input/Output VSWR Versus Frequency

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE5205 we have chosen an output level of −10.5dBm with fundamental frequencies of 100.000 and 100.01 MHz, respectively.

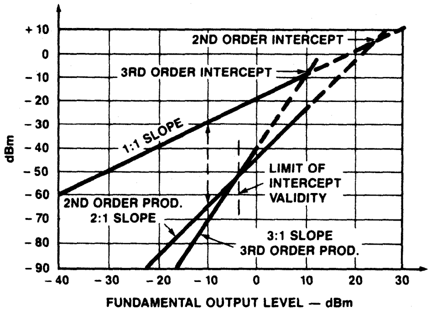


Figure 22

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers* by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

S-Parameter Techniques for Faster, More Accurate Network Design, H.P. App Note 95-1, Richard W. Anderson, 1967, HP Journal.

S-Parameter Design, H.P. App Note 154, 1972.

Section 7
Professional Analogue ICs

INDEX

MAINTENANCE TYPE LIST

The types listed below are not included in this handbook. Detailed information will be supplied on requested.

CA3046
TBA673
TBA915G
TCA210; T
TCA220
TCA240; D
TCA280A
TCA770A; D
TCA980G
TDA1024
TDA3081
TDA3083; D
TEA1010; T
TEA1016
TEA1058; T

STEPPING MOTOR DRIVE CIRCUIT

GENERAL DESCRIPTION

The SAA1027 is a bipolar integrated circuit intended for driving a four-phase two-stator motor. The circuit consists of a bidirectional four-state counter and a code converter to drive the four outputs in the sequence required for driving a stepping motor.

Features

- high noise immunity inputs
- clockwise and counter-clockwise operation
- reset facility
- high output current
- outputs protected against damage by overshoot.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		9,5 to 18	V
Supply current, unloaded	I_{CC}	typ.	4,5	mA
Input voltage, all inputs				
HIGH	V_{IH}	min.	7,5	V
LOW	V_{IL}	max.	4,5	V
Input current, all inputs, LOW	I_{IL}	typ.	30	μA
Output current LOW	I_{OL}	max.	500	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

7

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38A).

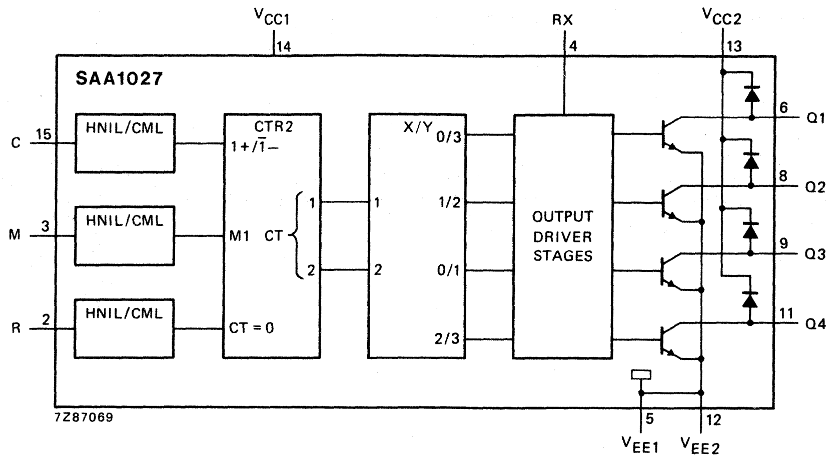


Fig. 1 Block diagram. The blocks marked HNIL/CML are high noise immunity input stages, the block marked CTR2 is a bidirectional synchronous 2-bit (4-state) counter and the block marked X/Y is a code converter. C is the count input, M the mode input to select forward or reverse counting and R is the reset input which resets the counter to content zero.

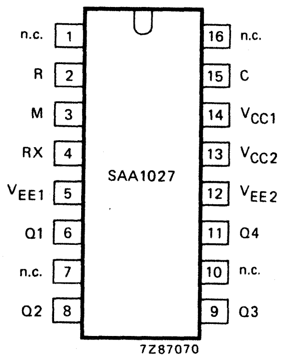


Fig. 2 Pinning diagram.

PINNING

1	n.c.	not connected
2	R	reset input
3	M	mode input
4	RX	external resistor
5	V_{EE1}	ground
6	Q1	output 1
7	n.c.	not connected
8	Q2	output 2
9	Q3	output 3
10	n.c.	not connected
11	Q4	output 4
12	V_{EE2}	ground
13	V_{CC2}	positive supply
14	V_{CC1}	positive supply
15	C	count input
16	n.c.	not connected

FUNCTIONAL DESCRIPTION

Count input C (pin 15)

The outputs change state after each L to H signal transition at the count input.

Mode input M (pin 3)

With the mode input the sequence of output signals, and hence the direction of rotation of the stepping motor, can be chosen, as shown in the following table.

counting sequence	M = L				M = H			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
0	L	H	L	H	L	H	L	H
1	H	L	L	H	L	H	H	L
2	H	L	H	L	H	L	H	L
3	L	H	H	L	H	L	L	H
0	L	H	L	H	L	H	L	H

Reset input R (pin 2)

A LOW level at the R input resets the counter to content zero. The outputs take on the levels shown in the upper and lower line of the table above.

If this facility is not used the R input should be connected to the supply.

External resistor pin RX (pin 4)

The external resistor R4 connected to RX sets the base current of the output transistors. Its value has to be chosen in accordance with the required output current (see Fig. 5).

Outputs Q1 to Q4 (pins 6, 8, 9 and 11)

The circuit has open-collector outputs. To prevent damage by an overshooting output voltage the outputs are protected by diodes connected to V_{CC2}, pin 13. High output currents mainly determine the total power dissipation, see Fig. 3.

7

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC1}; V_{CC2}	max.	18 V
Input voltage, all inputs	V_I	max.	18 V
Current into pin 4	I_{RX}	max.	120 mA
Output current	I_{OL}	max.	500 mA
Power dissipation	P_{tot}	see Fig. 4	
Storage temperature range	T_{stg}		−40 to +125 °C
Operating ambient temperature range	T_{amb}		−20 to +70 °C

CHARACTERISTICS

V_{CC} = 9,5 to 18 V; V_{EE} = 0 V; T_{amb} = −20 to 70 °C unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC1} and V_{CC2} (pins 14 and 13)					
Supply current at V_{CC1} = 12 V; unloaded; all inputs HIGH; pin 4 open	I_{CC}	2	4,5	6,5	mA
Inputs C, M and R (pins 15, 3 and 2)					
Input voltage					
HIGH	V_{IH}	7,5	–	–	V
LOW	V_{IL}	–	–	4,5	V
Input current					
HIGH	I_{IH}	–	1	–	μA
LOW	$-I_{IL}$	–	30	–	μA
External resistor pin RX (pin 4)					
Voltage at RX at V_{CC} = 12 V ± 15%; R4 = 130 Ω ± 5%	V_{RX}	3	–	4,5	V
Outputs Q1 to Q4					
Output voltage LOW					
at I_{OL} = 350 mA	V_{OL}	–	500	1000	mV
at I_{OL} = 500 mA	V_{OL}	–	700	–	mV
Output current					
LOW	I_{OL}	–	–	500*	mA
HIGH at V_Q = 18 V	$-I_{OH}$	–	–	50	μA

* See Figs 3 and 4.

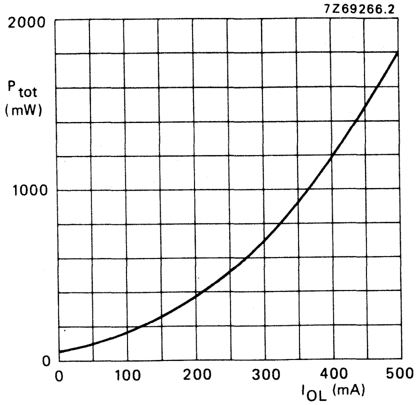


Fig. 3 Total power dissipation P_{tot} as a function of output current I_{OL}.

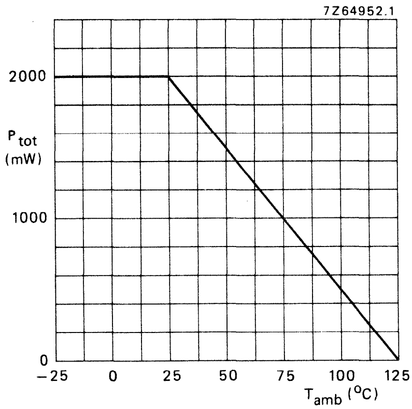


Fig. 4 Power derating curve.

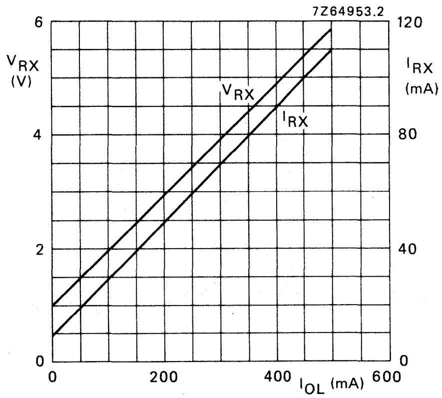


Fig. 5 Current I_{RX} into RX and voltage V_{RX} on RX as a function of required output current I_{OL}.

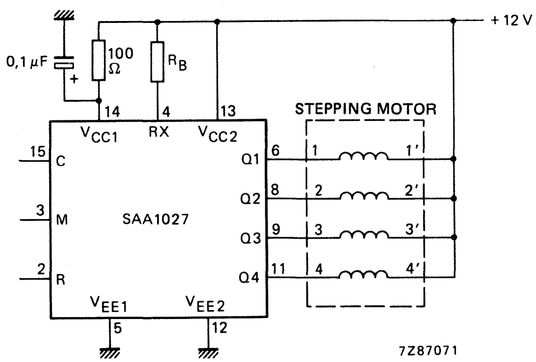


Fig. 6 Typical application of the SAA1027 as a stepping motor driver.

UNIVERSAL INDUSTRIAL LOGIC AND INTERFACE CIRCUIT

GENERAL DESCRIPTION

The SAA1029 is a universal bipolar logic and interface IC with high noise immunity and operational stability for industrial control applications. The most fundamental industrial control functions can be accomplished with only one SAA1029 IC. Figure 1 shows the logic configuration.

The IC comprises,
(1) Gate 1: 4-input AND gate with 1 inverted input,
(2) Gate 2: 3-input AND gate with 1 inverted input and adjustable propagation delay,
(3) Gate 3: 2-input AND gate with 1 inverted input.
The SAA1029 can be used as direct interface with LOCMOS (CMOS) ICs for realizing more complex functions. Therefore, the output signal can be limited to the voltage level of the common output clamping pin Z.

The propagation delay of NAND gate 2 is adjustable from microseconds to seconds by using an external capacitor at pin C. This makes it possible to adapt the control frequency limits to the system, so the optimum dynamic noise immunity can be achieved.

All the static and dynamic circuit values (including the output voltage) are independent of the supply voltage over a wide operating range. This allows the use of a simple unstabilized power supply.

The output is held to the LOW state automatically during switching on the power supply, so a special reset pulse can be omitted.

Features

- Simple realization of the basic industrial control functions (logic functions, timing functions, memory functions).
- High dynamic and static noise immunity.
- High operation stability.
- Short-circuit protection of inputs and outputs to both V_{EE} and V_{CC}.
- Wide supply voltage range, so a simple power supply can be used.
- Wire interruption results in a safe input LOW state.
- LOCMOS (CMOS) compatible.

7

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		14 to 31,2	V
Operating ambient temperature range	T_{amb}		−30 to + 85	°C
Input voltage HIGH	V_{IH}		6,5 to 44	V
Output voltage HIGH (without clamping)	V_{OH}		13 to 30	V
Output voltage HIGH (with clamping at pin Z)	V_{OH}		2,0 to (V_{CC} −0,7)	V
Input current	I_I	max.	10	mA
Quiescent supply current	I_{CC}	typ.	7,8	mA

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

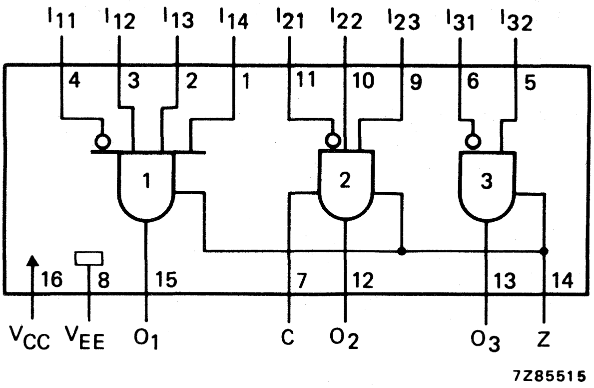


Fig. 1 Logic diagram.

Logic equations:

$O_1 = \overline{I_{11}} \cdot I_{12} \cdot I_{13} \cdot I_{14}$

$O_2 = \overline{I_{21}} \cdot I_{22} \cdot I_{23}$

$O_3 = \overline{I_{31}} \cdot I_{32}$

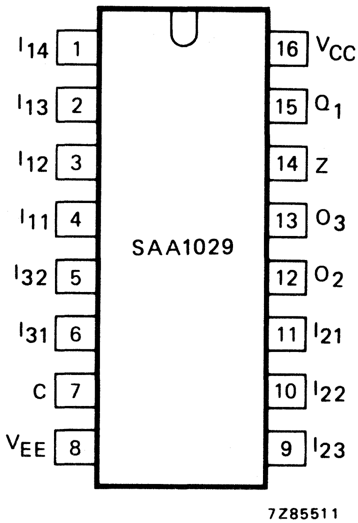


Fig. 2 Pinning diagram.

PINNING

4	I_{11}	inputs of gate 1
3	I_{12}	
2	I_{13}	
1	I_{14}	
15	O_1	output of gate 1
11	I_{21}	inputs of gate 2
10	I_{22}	
9	I_{23}	
12	O_2	output of gate 2
6	I_{31}	inputs of gate 3
5	I_{32}	
13	O_3	output of gate 3
7	C	external delay capacitor
14	Z	common output clamping
16	V_{CC}	positive supply voltage
8	V_{EE}	ground

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{CC}		0 to + 35	V
Input voltage (independent of V_{CC})	V_I		–0,15 to + 44	V
Output clamping voltage (pin 14)	V_Z		0 to + 35	V
Voltage at any output (pins 12, 13 and 15)				
pin 14 (Z) open	V_O		–0,15 to V_{CC}	V
pin 14 (Z) at V_Z	V_O	max.	V_Z	V
		or V_{CC} if $V_{CC} < V_Z$		
Current into any input				
d.c.	$\pm I_I$	max.	10	mA
t_p = 0,5 μs; δ = 0,1% (peak value)	$\pm I_{IM}$	max.	100	mA
Sum of input currents				
d.c.	ΣI_I		–90 to + 10	mA
t_p = 0,5 μs; δ = 0,1% (peak value)	ΣI_{IM}		–900 to + 300	mA
External applied current at any output (pins 12, 13 and 15)				
pin 14 (Z) open				
d.c.	$\pm I_O$	max.	30	mA
t_p = 0,5 μs; δ = 0,1% (peak value)	$\pm I_{OM}$	max.	500	mA
External applied current at any output (pins 12, 13 and 15)				
pin 14 (Z) at V_Z				
d.c.	I_O		–30 to + 10	mA
t_p = 0,5 μs; δ = 0,1% (peak value)	I_O		–500 to + 100	mA
Voltage at pin 7 (C)	V_C		–0,15 to + 6	V
External capacitor at pin 7 (C)	any value			
Short-circuit of outputs (pins 12, 13 and 15)				
pin 14 (Z) open	allowed to V_{CC} and V_{EE} (0 V)			
at $V_Z < V_{CC}$	allowed only to V_{EE} (0 V)			
Total power dissipation (see also Fig. 3)				
at T_{amb} = 50 °C; continuous	P_{tot}	max.	1100	mW
at T_{amb} = 65 °C; max. 1000 hours	P_{tot}	max.	1100	mW
Storage temperature range	T_{stg}		–40 to + 150	°C

7

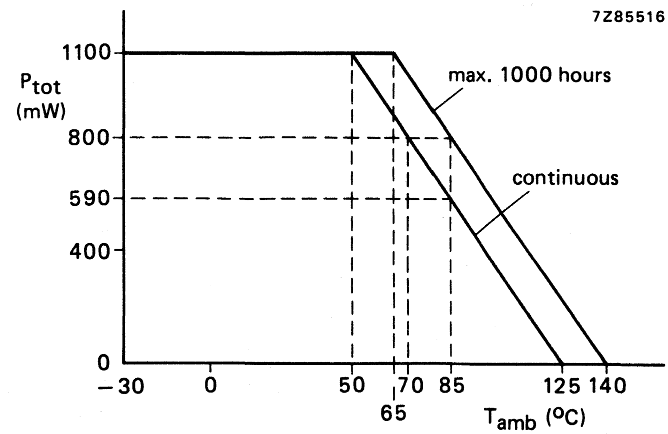


Fig. 3 Power derating curves; $R_{th\ j\text{-}a}$ = 70 K/W.

CHARACTERISTICS

At T_{amb} = −30 to + 85 °C; $T_j \leqslant 125$ °C; V_{CC} = 14 to 31,2 V; unless otherwise specified

	symbol	min.	typ.	max.	unit	conditions
Supply voltage	V_{CC}	14	24	31,2	V	
Quiescent supply current	I_{CC}	–	7,8	–	mA	
	I_{CC}	–	–	12,2	mA	V_{CC} = 31 V; T_{amb} = 25 °C
Quiescent current ratio	$\frac{I_{CC1}}{I_{CC2}}$	–	0,67	–		$I_{CC1} = I_{CC}$ at T_j = 125 °C $I_{CC2} = I_{CC}$ at T_j = 25 °C
Input voltage LOW	V_{IL}	–	–	5	V	
Input voltage HIGH	V_{IH}	6,5	–	–	V	
	V_{IH}	6,55	–	–	V	
Input current LOW	$-I_{IL}$	–	–	100	μA	
	$-I_{IL}$	–	–	95	μA	
Input current HIGH	I_{IH}	300	–	–	μA	
Rate of change of input signal	dV/dt	3	–	–	V/ms	
Input current*	$-I_I$	–	–	120	μA	V_I = 1 V
	I_I	–	–	280	μA	V_I = 35 V
Output clamping voltage*	V_Z	–	–	30	V	$V_Z = V_{CC}$ −1 V
Output voltage without clamping (pin 14 open)* non-inverting input: V_I = 5,1 V inverting input: V_I = 6,3 V						V_{CC} = 14 V
LOW	V_{OL}	–	–	1	V	I_O = 1,32 mA
	V_{OL}	–	–	1,5	V	I_O = 2,91 mA
HIGH	V_{OH}	V_{CC}−1,4	–	–	V	$-I_O$ = 5 mA
Output voltage with clamping (pin 14 at V_Z)*						V_{CC} = 31,2 V $V_Z < V_{CC}$−1 V
LOW	V_{OL}	–	–	1	V	I_O = 1,32 mA
	V_{OL}	–	–	1,5	V	I_O = 1,91 mA

HIGH	V_{OH}	$(V_Z -0,475)$	–	$(V_Z +0,225)$	V	$I_O = 0$ mA
	V_{OH}	$(V_Z -0,455)$	–	$(V_Z +0,12)$	V	$-I_O = 1$ mA
	V_{OH}	$(V_Z -0,41)$	–	$(V_Z +0,055)$	V	$-I_O = 3$ mA
Output short-circuit current*						
LOW-signal	I_{OscL}	2,95	–	9,6	mA	output at V_{CC}
HIGH-signal	$-I_{OscH}$	10,1	–	21,9	mA	output at V_{EE} (0 V)
Capacitor charging current*	I_C	–	30	–	μA	
Propagation delays*						
gates 1, 2 and 3						
HIGH to LOW	t_{PHL}	–	3,5	–	μs	C = 0 (at gate 2)
LOW to HIGH	t_{PLH}	–	3,5	–	μs	
gate 2						
HIGH to LOW	t_{PHL}	1,85	–	5,2	ms	C = 47 nF ± 1%
LOW to HIGH	t_{PLH}	7,5	–	14	ms	$R_{insulation} > 100$ MΩ

* At $T_{amb} = 25$ °C; $V_{CC} = 24$ V; unless otherwise specified.

CHARACTERISTICS (worst case conditions)

At T_j = + 125 to + 140 °C; maximum 1000 hours

	symbol	min.	typ.	max.	unit	conditions
Input voltage LOW	V_{IL}	–	–	5	V	
Input voltage HIGH	V_{IH}	6,55	–	–	V	
Input current	I_I	95	–	300	μA	V_I = 1 to 44 V
Change of input current overdrive of other inputs $\Sigma(-I_I) < 10$ mA	ΔI_I	–	–	120	μA	$V_I < V_{CC} - 1$ V
	ΔI_I	–	–	158	μA	$V_I > V_{CC} - 1$ V
overdrive of other inputs $\Sigma(-I_I) < 90$ mA	ΔI_I	–	–	280	μA	$V_I < V_{CC} - 1$ V
	ΔI_I	–	–	320	μA	$V_I > V_{CC} - 1$ V
Input voltage by current overdrive	V_I	46	–	65	V	$\Sigma(-I_I)$ = 10 mA
Output voltage without clamping (pin 14 open) LOW	V_{OL}	–	–	0,35	V	$I_{OL} \leqslant 0{,}095$ mA
	V_{OL}	–	–	1	V	I_{OL} = 0,095 to 1 mA
	V_{OL}	–	–	1,5	V	I_{OL} = 1 to 2,5 mA
HIGH	V_{OH}	$V_{CC}-1{,}5$	–	–	V	$-I_{OH} \leqslant 5$ mA
Output voltage with clamping (pin 14 at V_Z)						V_Z = 2,5 to $V_{CC} - 1$ V
HIGH	V_{OH}	$(V_Z - 0{,}5)$	–	$(V_Z + 0{,}245)$	V	I_{OH} = 0 mA
	V_{OH}	$(V_Z - 0{,}5)$	–	$(V_Z + 0{,}15)$	V	I_{OH} = 1 mA
	V_{OH}	$(V_Z - 0{,}5)$	–	V_Z	V	I_{OH} = 3 mA
	V_{OH}	–	–	0,75	V	I_{OH} = 0 mA; V_Z = 0 V
Output short-circuit current LOW-signal	I_{OscL}	–	–	11	mA	output at V_{CC}
HIGH-signal	$-I_{OscH}$	5	–	28,5	mA	output at V_{EE} (0 V)
HIGH-signal	$-I_{OscH}$	–	–	10	mA	output at V_{EE} (0 V); T_j = 140 °C

Current out of pin 14 (Z) when currents are	$-I_Z$	–	–	2,2	mA	$-I_O \leqslant 3$ mA
forced into outputs	$-I_Z$	ΣI_O	–	–	mA	$\Sigma I_O = (I_{O1} + I_{O2} + I_{O3})$
Current into pin 14 (Z) when inputs are set for output to be LOW	I_Z	–	–	300	μA	$-I_O = 30$ mA; $V_O \leqslant V_{EE}$
Supply current change	ΔI_{CCmax}	$(0,3 \times \lvert I_I \rvert) + (0,55 \times \lvert I_O \rvert)$			mA	input and/or output voltages are negative with respect to V_{EE}
Propagation delays						
gates 1 and 3						
HIGH to LOW	t_{PHL}	1	–	7	μs	
LOW to HIGH	t_{PLH}	1	–	7	μs	
gate 2						
HIGH to LOW	t_{PHL}	0,1	–	4	μs	without capacitor
LOW to HIGH	t_{PLH}	0,3	–	6	μs	without capacitor
HIGH to LOW	t_{PHL}	38 x C	–	113 x C	μs	with capacitor; C in μF
LOW to HIGH	t_{PLH}	142 x C	–	334 x C	μs	with capacitor; C in μF
Voltage spikes output LOW	V_{OL}	–	–	2	V	see note

Note

V_{CC} rising from 0 to 14 V; all inputs open; internally it is guaranteed that the input threshold voltage $V_{IL} > V_{OL}$.

APPLICATION INFORMATION

The following figures (Figs 4 to 11) give some examples of the basic industrial control functions.

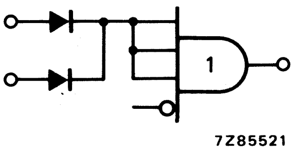


Fig. 4 OR function.

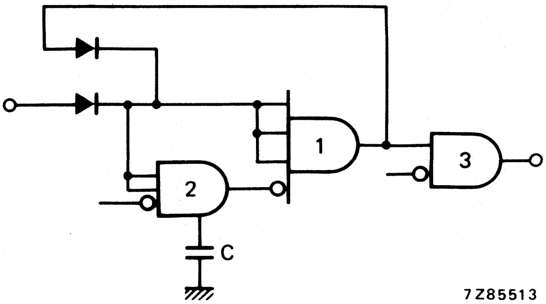


Fig. 8 Monostable flip-flop; for C = 4,7 μF, 1 s no reaction.

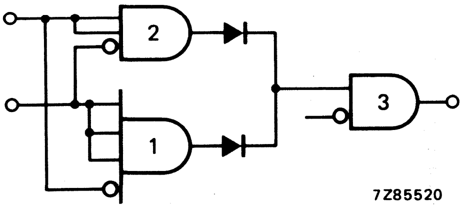


Fig. 5 EXCLUSIVE-OR function.

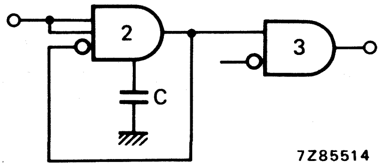


Fig. 9 Start delay function.

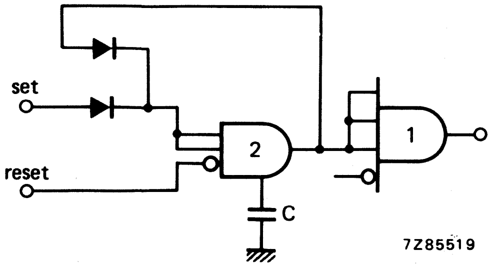


Fig. 6 Delayed memory; reset is dominating.

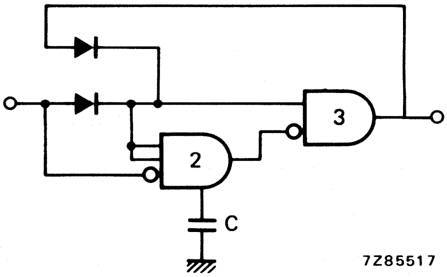


Fig. 10 Decay delay function.

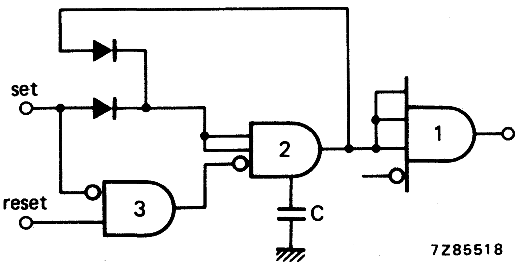


Fig. 7 Delayed memory; set is dominating.

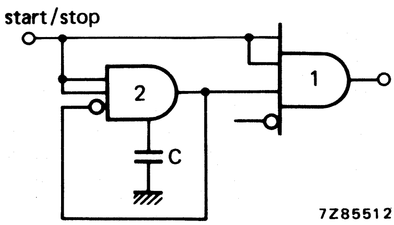


Fig. 11 Square-wave oscillator.

OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The TCA520 is a bipolar integrated operational amplifier primarily intended for low-power, low-voltage applications and as a comparator in digital systems.

Features

- wide supply voltage range
- low supply voltage operation
- low power consumption
- low input bias current
- offset compensation facility
- frequency compensation facility
- high slew rate
- large output voltage swing
- TTL compatible output

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		2 to 20	V
Supply current	I_{CC}	typ.	0,8	mA
Input bias current	I_{IB}	typ.	60	nA
Output voltage range	V_O		0,1 to V_{CC}–0,1	V
D.C. differential voltage amplification	A_{VD}	typ.	15 000	
Slew rate	S_{VOAV}	typ.	25	V/μs
Operating ambient temperature range	T_{amb}		–25 to + 85	°C

7

PACKAGE OUTLINES

TCA520B : 8-lead DIL; plastic (SOT-97A).
TCA520D: 8-lead mini-pack; plastic (SO-8; SOT-96A).

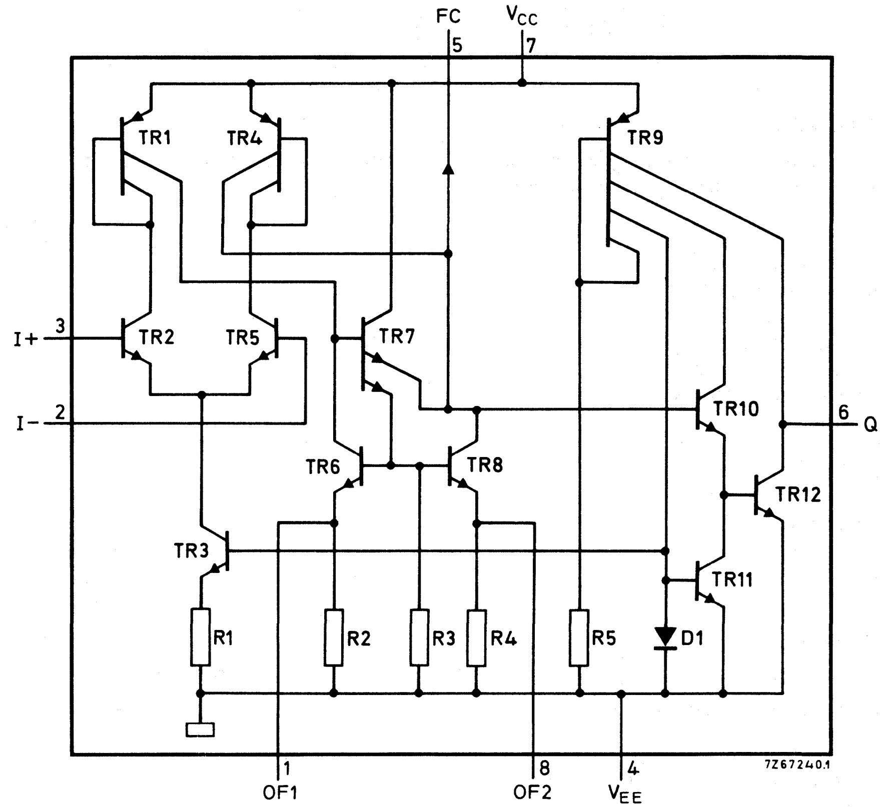


Fig. 1 Circuit diagram.

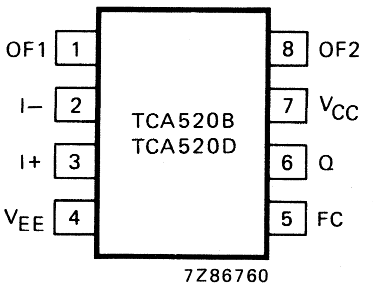


Fig. 2 Pinning diagram.

PINNING

1	OF1	offset compensation connection
2	I−	inverting input
3	I+	non-inverting input
4	V_{EE}	ground connection
5	FC	frequency compensation connection
6	Q	output
7	V_{CC}	positive supply connection
8	OF2	offset compensation connection

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC}	max.	22 V
Input voltage	V_I	max.	V_{CC} V
	$-V_I$	max.	0 V
Differential input voltage	$\pm V_{ID}$	max.	7 V
Power dissipation at T_{amb} = 85 °C	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}		−55 to + 125 °C
Operating ambient temperature range	T_{amb}		−25 to + 85 °C

CHARACTERISTICS

V_{CC} = 5 V; V_{EE} = 0 V; T_{amb} = 25 °C; R_L from Q to V_{CC} unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC}; pin 7					
Supply current, unloaded	I_{CC}	0,5	0,8	1,2	mA
Inputs I+ and I−; pins 3 and 2					
Input voltage	V_I	0,9	–	V_{CC}−0,5	V
Input bias current	I_{IB}	–	60	250	nA
Input offset voltage	V_{IO}	–	1	6	mV
Variation with temperature	ΔV_{IO}	–	5	–	μV/K
Input offset current	I_{IO}	–	10	75	nA
Common-mode rejection ratio	k_{CMR}	70	100	–	dB
Input noise voltage at f = 1 kHz	$V_{n(rms)}$	–	15	–	$nV/\sqrt{Hz}$
Input noise current at f = 1 kHz	$I_{n(rms)}$	–	0,4	–	$pA/\sqrt{Hz}$
Output Q; pin 6					
Output voltage range at R_L = 5 kΩ	V_Q	0,1	–	V_{CC}−0,1	V
Output current					
HIGH at $V_Q = V_{CC} - 0,4$ V	$-I_{OH}$	100	200	–	μA
LOW at V_Q = 0,4 V	I_{OL}	6	12	–	mA
D.C. voltage amplification at R_L = 5 kΩ	A_{VD}	10 000	15 000	–	
A.C. voltage amplification at f = 1 kHz; C_{FC} = 100 pF	A_{vd}	–	58	–	dB
Slew rate (average rate of change of the output voltage) at R_L = 1 kΩ					
C_{FC} = 0 pF	S_{VOAV}	–	25	–	V/μs
C_{FC} = 100 pF	S_{VOAV}	–	500	–	mV/μs

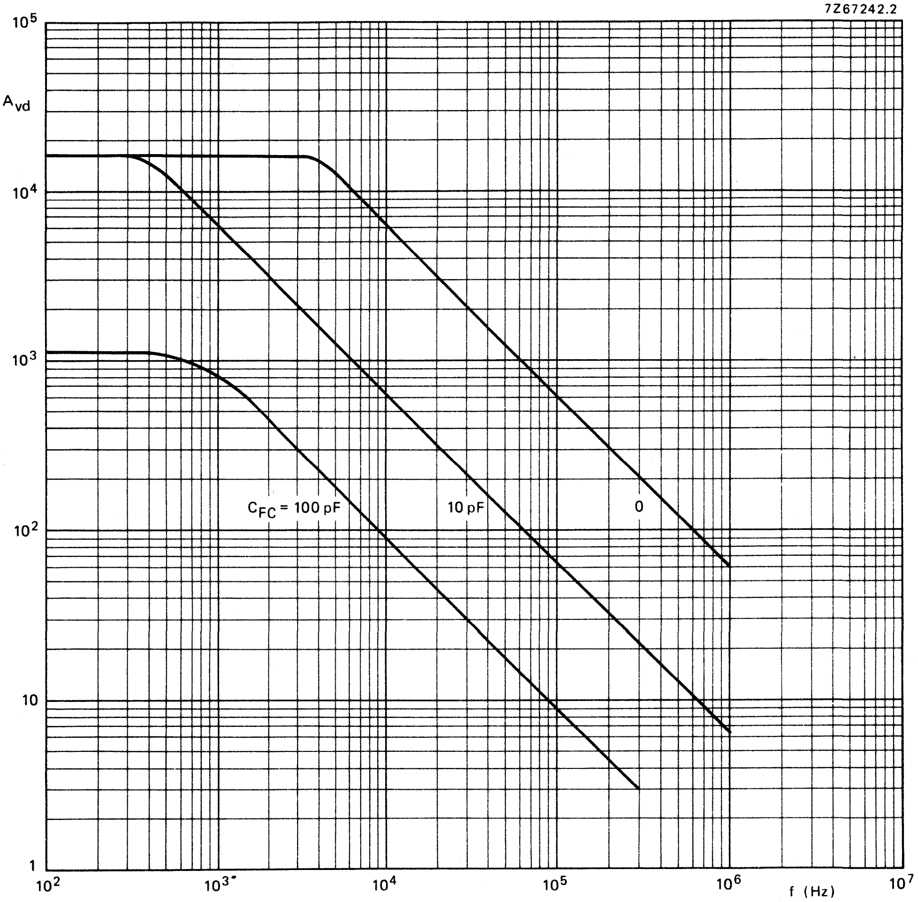


Fig. 3 Typical values of the open-loop voltage amplification as a function of frequency.

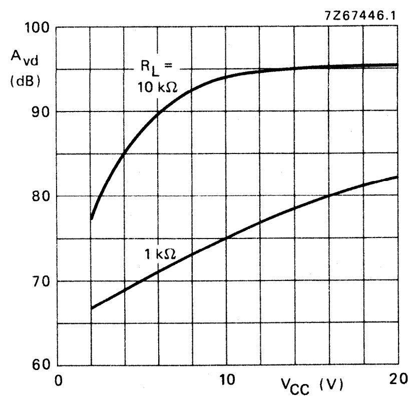


Fig. 4 Typical values of the open-loop voltage amplification as a function of supply voltage.

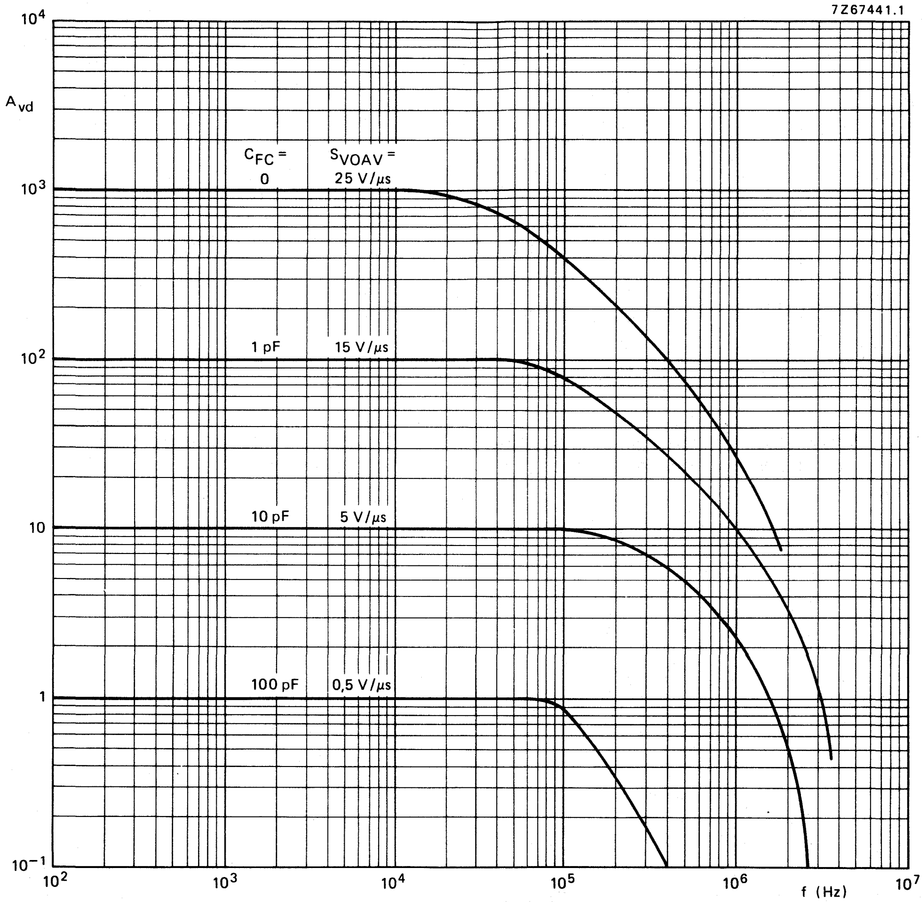


Fig. 5 Typical frequency response and slew rate for various closed-loop gains.

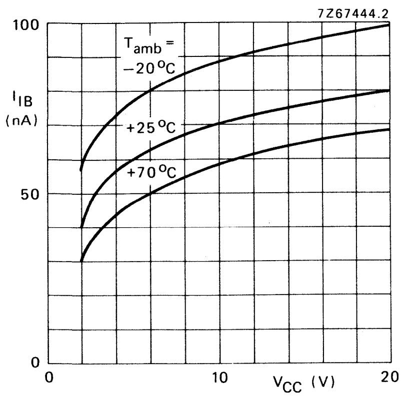


Fig. 6 Typical values of the input bias current as a function of supply voltage, with ambient temperature as a parameter.

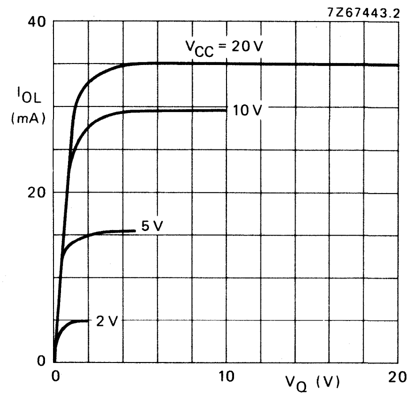


Fig. 7 Output current LOW as a function of output voltage, with supply voltage as a parameter.

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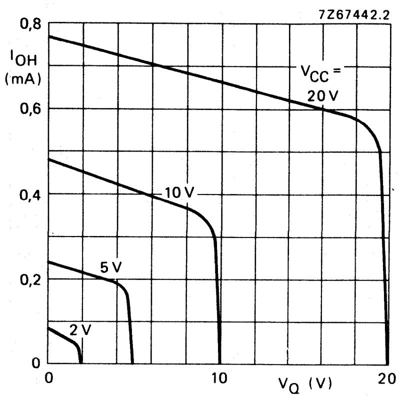

Fig. 8 Output current HIGH as a function of output voltage, with supply voltage as a parameter.

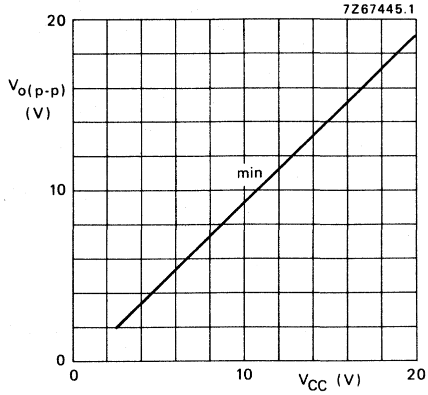

Fig. 9 Minimum values of the output voltage swing as a function of supply voltage for R_L = 1 kΩ.

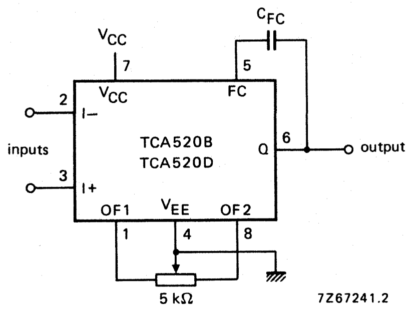

Fig. 10 Typical arrangement of the TCA520 with frequency and offset compensation.

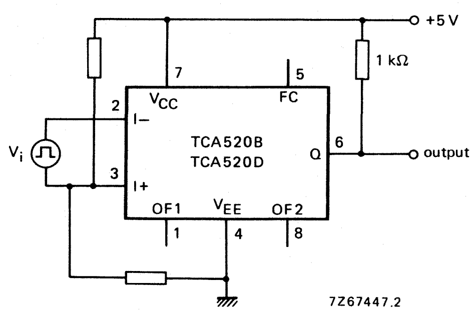

Fig. 11 Typical application of the TCA520 as a comparator.

PROPORTIONAL-CONTROL TRIAC TRIGGERING CIRCUIT

GENERAL DESCRIPTION

The TDA1023 is a bipolar integrated circuit for controlling triacs in the time proportional or burst firing mode. It permits very precise temperature control of heating equipment and is especially suited for the control of panel heaters. The circuit generates positive-going trigger pulses and complies with the regulations on radio interference and mains distortion.

Special features are:

- adjustable proportional range width
- adjustable hysteresis
- adjustable trigger pulse width
- adjustable firing burst repetition time
- control range translation facility
- failsafe operation
- supplied from the mains
- provides supply for external temperature bridge

QUICK REFERENCE DATA

Supply voltage (derived from mains voltage)	V_{CC}	typ.	13,7	V
Stabilized supply voltage for temperature bridge	V_Z	typ.	8	V
Supply current (average value)	$I_{16(AV)}$	typ.	10	mA
Trigger pulse width	t_w	typ.	200	μs
Firing burst repetition time at $C_T = 68\ \mu F$	T_b	typ.	41	s
Output current	$-I_{OH}$*	max.	150	mA
Operating ambient temperature range	T_{amb}		−20 to + 75	°C

* Negative current is defined as conventional current flow out of a device. A negative output current is suited for positive triac triggering.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

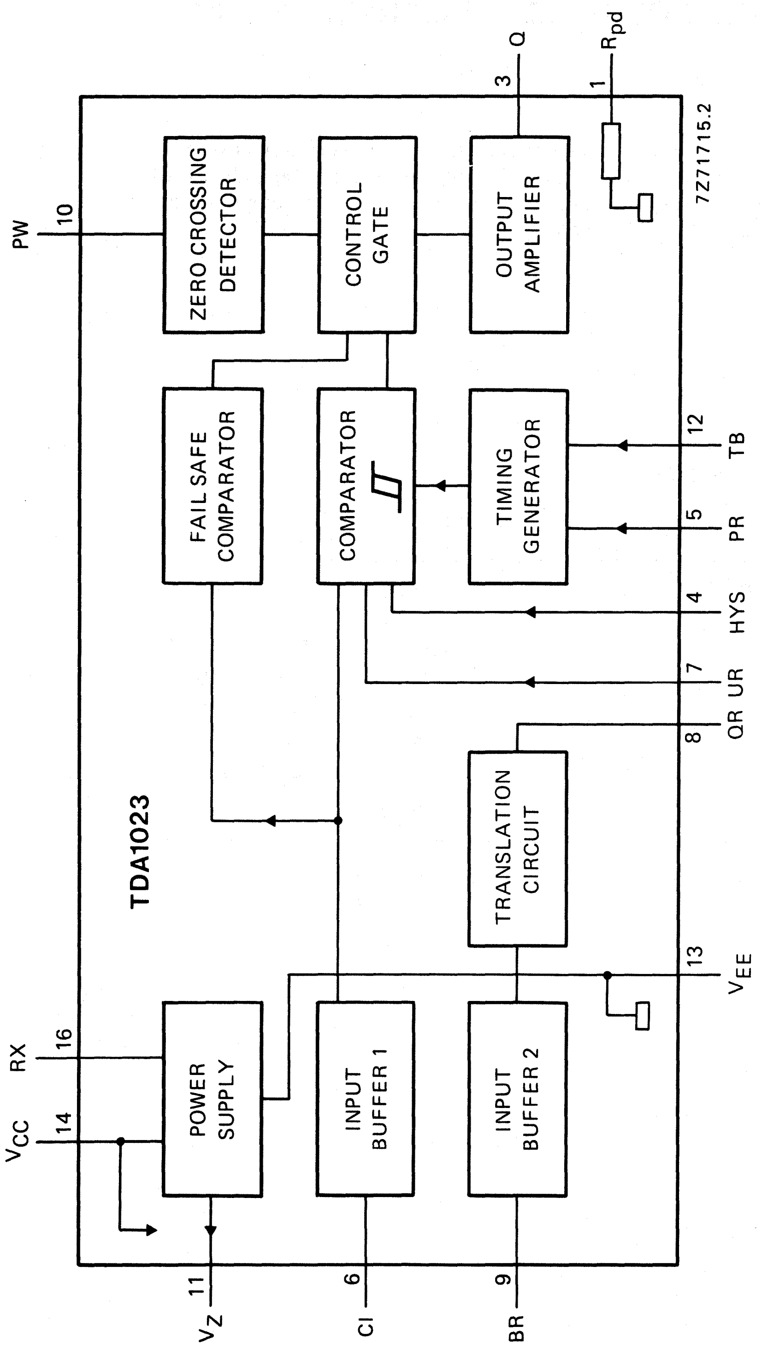

Fig. 1 Block diagram.

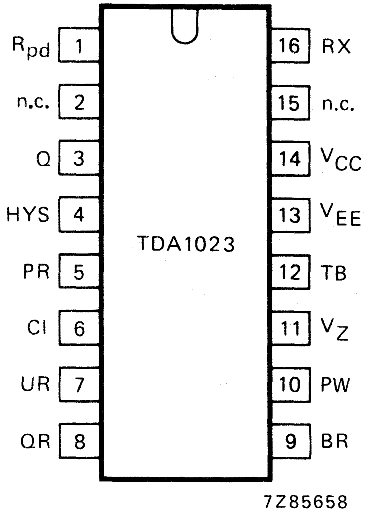

Fig. 2 Pinning diagram.

PINNING

1	R_{pd}	internal pull-down resistor connection
2	n.c.	not connected
3	Q	output
4	HYS	hysteresis control input
5	PR	proportional range control input
6	CI	Control input
7	UR	unbuffered reference input
8	QR	output of reference buffer
9	BR	buffered reference input
10	PW	pulse width control input
11	V_Z	reference supply output
12	TB	firing burst repetition time control input
13	V_{EE}	ground connection
14	V_{CC}	positive supply connection
15	n.c.	not connected
16	RX	external resistor connection

FUNCTIONAL DESCRIPTION

The TDA1023 generates pulses to trigger a triac. These trigger pulses coincide with the zero crossings of the mains voltage. This minimizes r.f. interference and transients on the mains supply. The trigger pulses come in bursts, with the net effect that the load is periodically switched on and off. This further minimizes mains pollution. The average power in the load is varied by varying the duration of the trigger pulse burst, in accordance with the voltage difference between the control input CI and the reference input, either UR or BR.

Power supply: V_{CC}, RX and V_Z (pins 14, 16 and 11)

The TDA1023 is supplied from the a.c. mains via a resistor R_D to the RX connection (pin 16); the V_{EE} connection (pin 13) is connected to the neutral line (see Fig. 4a). A smoothing capacitor C_S has to be connected between the V_{CC} and V_{EE} connections.

The circuit contains a string of stabilizer diodes between the RX and V_{EE} connections that limit the d.c. supply voltage, and a rectifier diode between the RX and V_{CC} connections (see Fig. 3).

At pin 11 the device provides a stabilized reference voltage V_Z for an external temperature sensing bridge.

The operation of the supply arrangement is as follows. During the positive half of the mains cycles the current through external voltage dropping resistor R_D charges the external smoothing capacitor C_S until RX reaches the stabilizing voltage of the internal stabilizer diodes. R_D should be chosen such that it can supply the current I_{CC} for the TDA1023 itself plus the average output current $I_{3(AV)}$ plus the current required from the V_Z connection for an external temperature bridge, and recharge the smoothing capacitor C_S (see Figs 9 to 12). Any excess current is bypassed by the internal stabilizer diodes. Note that the maximum rated supply current must not be exceeded.

During the negative half of the mains cycles external smoothing capacitor C_S has to supply the sum of the currents mentioned above. Its capacitance must be high enough to maintain the supply voltage above the minimum specified limit.

FUNCTIONAL DESCRIPTION (continued)

Dissipation in resistor R_D is halved by connecting a diode in series (see Fig. 4b and 9 to 12).

A further reduction of dissipation is possible by using a high-quality voltage dropping capacitor C_D in series with a resistor R_{SD} (see Figs 4c and 14). Asuitable VDR connected across the mains provides protection of the TDA1023 and of the triac against mains-borne transients.

Control and reference inputs CI, BR and UR (pins 6, 9 and 7)

For room temperature control (5 °C to 30 °C) the best performance is obtained by using the translation circuit. The buffered reference input BR (pin 9) is used as a reference input, and the output of the reference buffer QR (pin 8) is connected to the unbuffered reference input UR (pin 7). In this arrangement the translation circuit ensures that most of the potentiometer rotation can be used to cover the room temperature range. This provides an accurate temperature setting and a linear temperature scale.

If the translation circuit is not required, the unbuffered reference input UR (pin 7) is used as a reference input. The buffered reference input BR (pin 9) must be connected to the reference supply output V_Z (pin 11).

For proportional power control the unbuffered reference input UR (pin 7) must be connected to the firing burst repetition time control input TB (pin 12) and the buffered reference input BR (pin 9), which is inactive now, must be connected to the reference supply output V_Z (pin 11).

In all arrangements the train of output pulses becomes longer when the voltage at the control input CI (pin 6) becomes lower.

Proportional range control input PR (pin 5)

With the proportional range control input PR open the output duty factor changes from 0% to 100% by a variation of 80 mV at the control input CI (pin 6). For temperature control this corresponds with a temperature difference of only 1 K.

This range may be increased to 400 mV, i.e. 5 K, by connecting the proportional range control input PR (pin 5) to ground. Intermediate values are obtained by connecting the PR input to ground via a resistor R5, see Table 1.

Hysteresis control input HYS (pin 4)

With the hysteresis control input HYS (pin 4) open the device has a built-in hysteresis of 20 mV. For temperature control this corresponds with 0,25 K.

Hysteresis is increased to 320 mV, corresponding with 4 K, by grounding HYS (pin 4). Intermediate values are obtained by connecting pin 4 to ground via a resistor R4. See Table 1 for a set of values for R4 and R5 giving a fixed ratio between hysteresis and proportional range.

Trigger pulse width control input PW (pin 10)

The trigger pulse width may be adjusted to the value required for the triac by choosing the value of the external synchronization resistor R_S between the trigger pulse width control input PW (pin 10) and the a.c. mains. The pulse width is inversely proportional to the input current (see Fig. 13).

Output Q (pin 3)

Since the circuit has an open-emitter output, it is capable of sourcing current, i.e. supplying a current out of the output. Therefore it is especially suited for generating positive-going trigger pulses. The output is current-limited and protected against short-circuits. The maximum output current is 150 mA and the output pulses are stabilized at 10 V for output currents up to that value.

FUNCTIONAL DESCRIPTION (continued)

A gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Figs 5 to 8). This minimizes the total supply current and the power dissipation.

Pull-down resistor R_{pd} (pin 1)

The TDA1023 includes a 1,5 kΩ pull-down resistor R_{pd} between pins 1 and 13 (V_{EE}, ground connection), intended for use with sensitive triacs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC}	max.	16	V
Supply current				
average	$I_{16(AV)}$	max.	30	mA
repetitive peak	$I_{16(RM)}$	max.	100	mA
non-repetitive peak	$I_{16(SM)}$	max.	2	A
Input voltage, all inputs	V_I	max.	16	V
Input current, CI, UR, BR, PW input	$I_{6; 7; 9; 10}$	max.	10	mA
Voltage on R_{pd} connection	V_1	max.	16	V
Output voltage, Q, QR, V_Z output	$V_{3; 8; 11}$	max.	16	V
Output current				
average	$-I_{OH(AV)}$	max.	30	mA
peak, max. 300 μs	$-I_{OH(M)}$	max.	700	mA
Total power dissipation	P_{tot}	max.	500	mW
Storage temperature range	T_{stg}	−55 to + 150		°C
Operating ambient temperature range	T_{amb}	−20 to + 75		°C

7

CHARACTERISTICS

V_{CC} = 11 to 16 V; T_{amb} = −20 to + 75 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply: V_{CC} and RX (pins 14 and 16)					
Internally stabilized supply voltage at I_{16} = 10 mA	V_{CC}	12	13,7	15	V
Variation with I_{16}	$\Delta V_{CC}/\Delta I_{16}$	–	30	–	mV/mA
Supply current at $V_{16\text{-}13}$ = 11 to 16 V; I_{10} = 1 mA; f = 50 Hz; pin 11 open; $V_{6\text{-}13} > V_{7\text{-}13}$; pins 4 and 5 open	I_{16}	–	–	6	mA
pins 4 and 5 grounded	I_{16}	–	–	7,1	mA
Reference supply output V_Z (pin 11) for external temperature bridge					
Output voltage	$V_{11\text{-}13}$	–	8	–	V
Output current	$-I_{11}$	–	–	1	mA
Control and reference inputs CI, BR and UR (pins 6, 9 and 7)					
Input voltage to inhibit the output	$V_{6\text{-}13}$	–	7,6	–	V
Input current at V_I = 4 V	$I_{6;\,7;\,9}$	–	–	2	µA
Hysteresis control input HYS (pin 4)					
Hysteresis, pin 4 open	ΔV_6	9	20	40	mV
pin 4 grounded	ΔV_6	–	320	–	mV
Proportional range control input PR (pin 5)					
Proportional range, pin 5 open	ΔV_6	50	80	130	mV
pin 5 grounded	ΔV_6	–	400	–	mV
Pulse width control input PW (pin 10)					
Pulse width at $I_{10(RMS)}$ = 1 mA; f = 50 Hz	t_w	100	200	300	µs
Firing burst repetition time control input TB (pin 12)					
Firing burst repetition time, ratio to capacitor C_T	T_b/C_T	320	600	960	ms/µF
Output of reference buffer QR (pin 8)					
Output voltage at input voltage $V_{9\text{-}13}$ = 1,6 V	$V_{8\text{-}13}$	–	3,2	–	V
$V_{9\text{-}13}$ = 4,8 V	$V_{8\text{-}13}$	–	4,8	–	V
$V_{9\text{-}13}$ = 8 V	$V_{8\text{-}13}$	–	6,4	–	V

	symbol	min.	typ.	max.	unit
Output Q (pin 3)					
Output voltage HIGH at $-I_{OH}$ = 150 mA	V_{OH}	10	–	–	V
Output current HIGH	$-I_{OH}$	–	–	150	mA
Internal pull-down resistor R_{pd} (pin 1)					
Resistance to V_{EE}	R_{pd}	1	1,5	3	kΩ

Table 1. Adjustment of proportional range and hysteresis.
Combinations of resistor values giving hysteresis > ¼ proportional range.

proportional range mV	proportional range resistor R5 kΩ	minimum hysteresis mV	maximum hysteresis resistor R4 kΩ
80	open	20	open
160	3,3	40	9,1
240	1,1	60	4,3
320	0,43	80	2,7
400	0	100	1,8

Table 2. Timing capacitor C_T values.

effective d.c. value	marked a.c. specification		catalogue number*
μF	μF	V	
68	47	25	2222 016 90129
47	33	40	– – 90131
33	22	25	– 015 90102
22	15	40	– – 90101
15	10	25	– – 90099
10	6,8	40	– – 90098

* Special electrolytic capacitors recommended for use with TDA1023.

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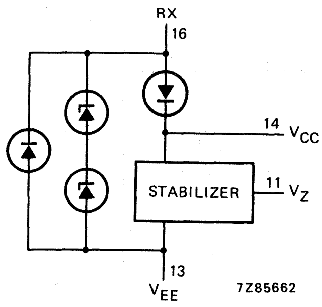

Fig. 3 Internal supply connections.

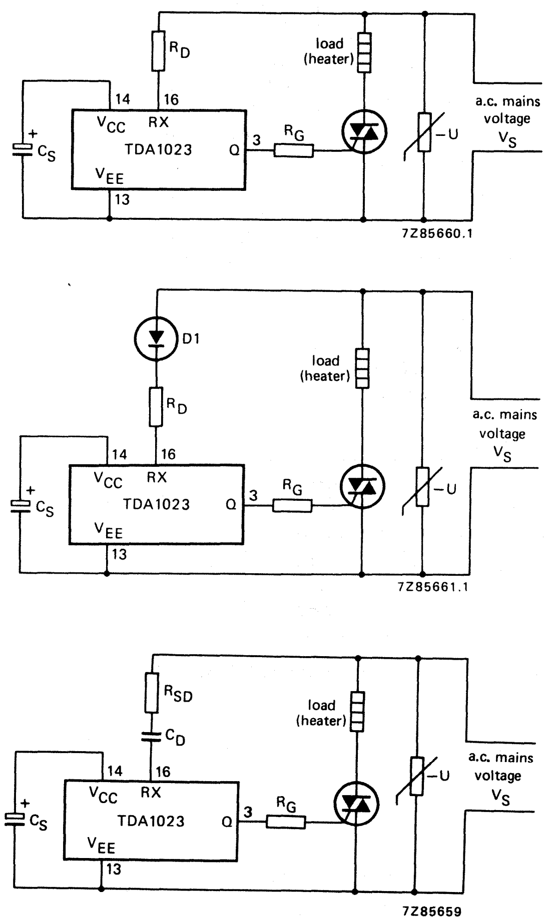

Fig. 4 Alternative supply arrangements.

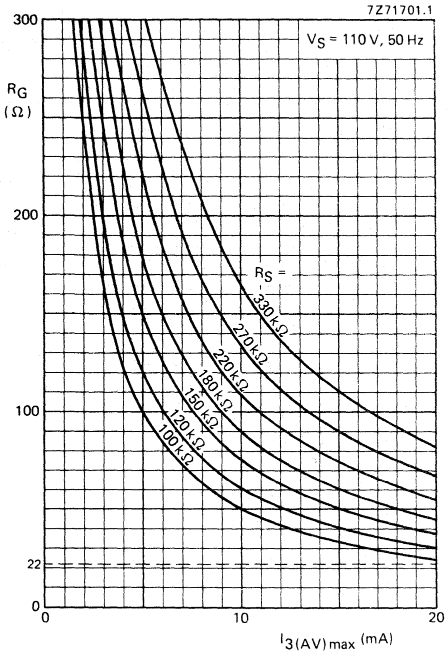

Fig. 5.

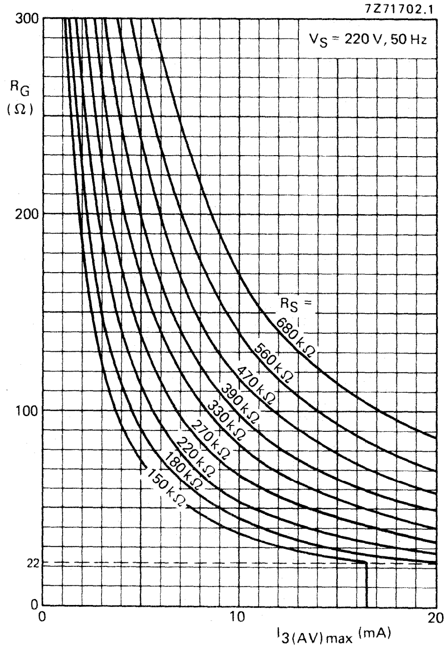

Fig. 6.

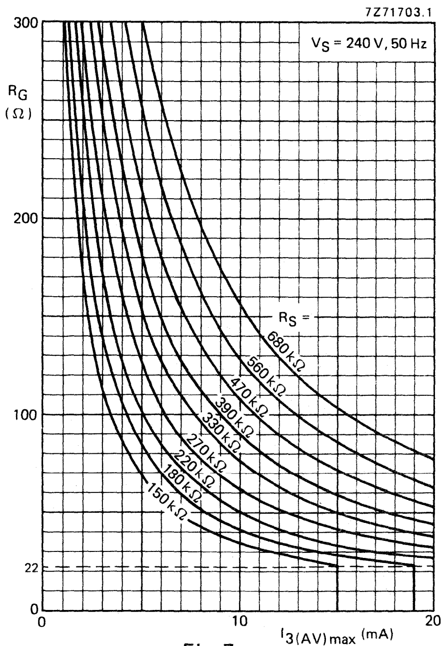

Fig. 7.

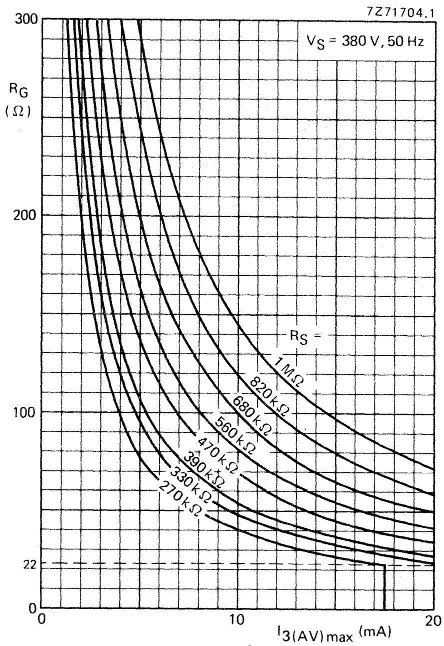

Fig. 8.

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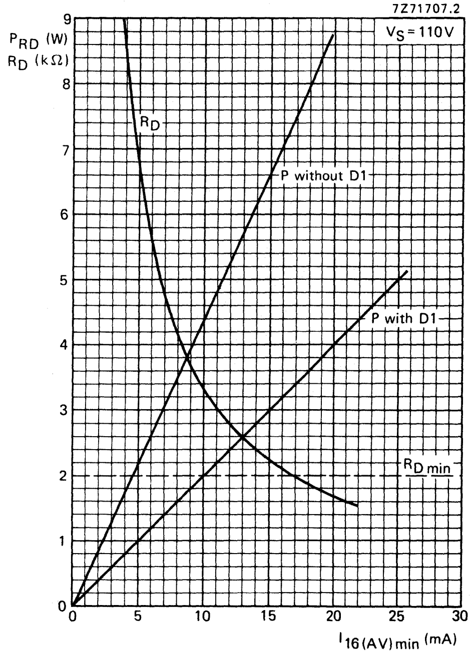

Fig. 9.

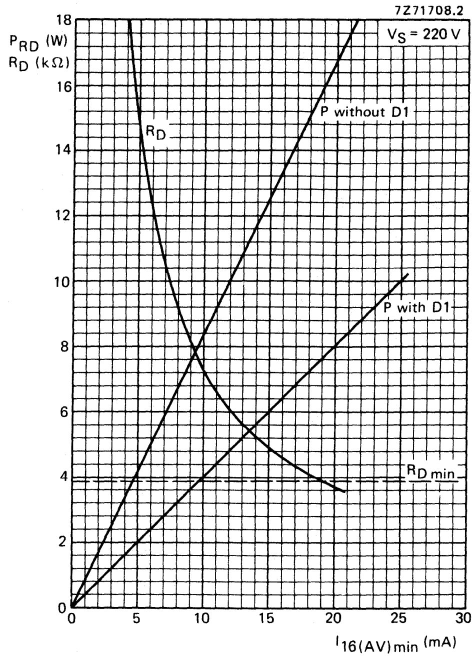

Fig. 10.

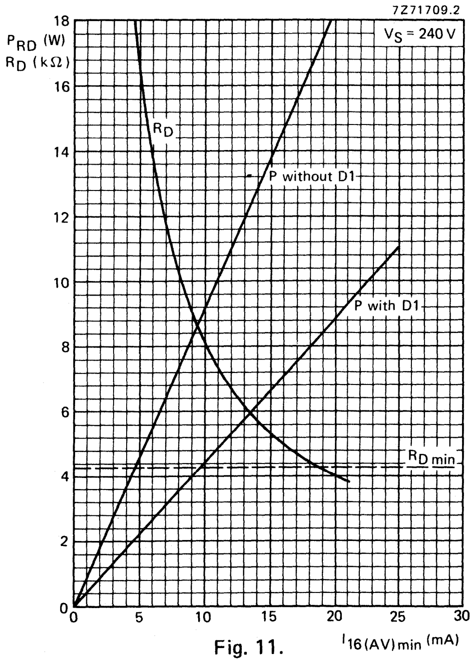

Fig. 11.

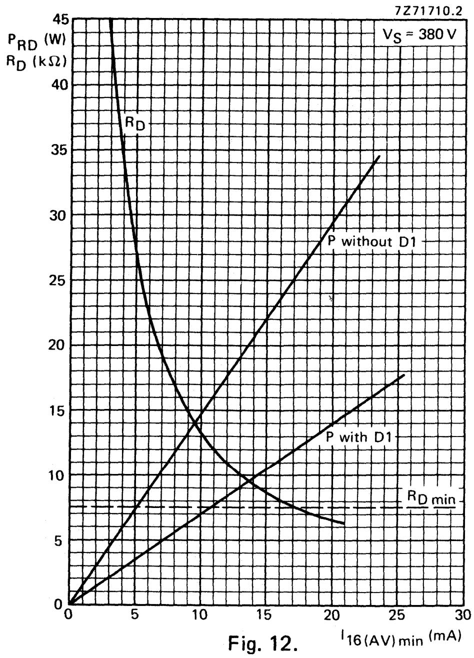

Fig. 12.

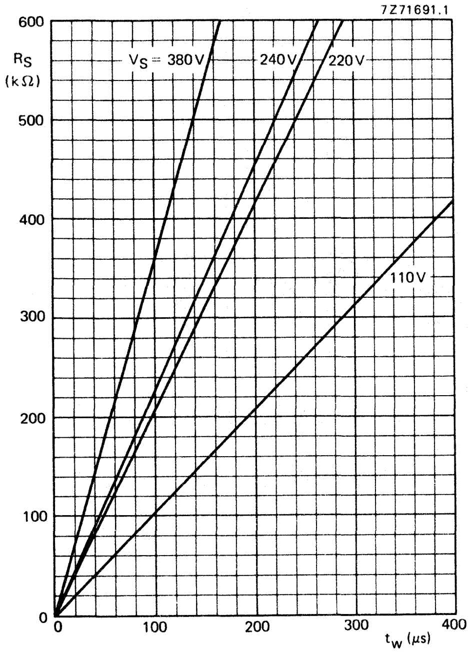

Fig. 13 Synchronization resistor R_S as a function of required trigger pulse width t_W with mains voltage V_S as a parameter.

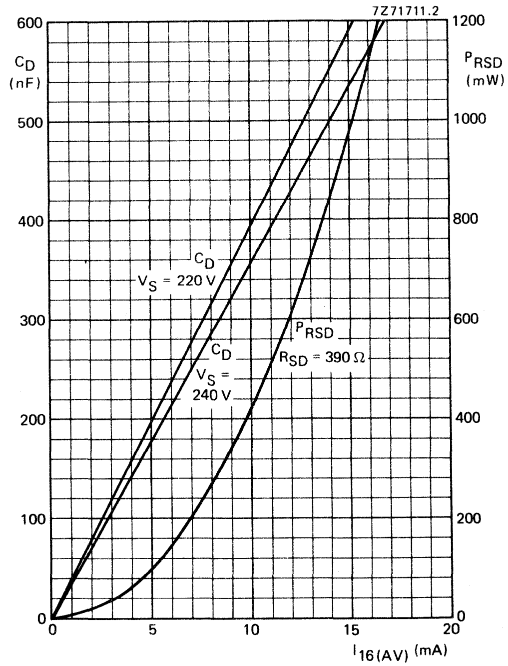

Fig. 14 Nominal value of voltage dropping capacitor C_D and power P_{RSD} dissipated in voltage dropping resistor R_{SD} as a function of the average supply current $I_{16(AV)}$ with the mains supply voltage V_S as a parameter.

APPLICATION INFORMATION

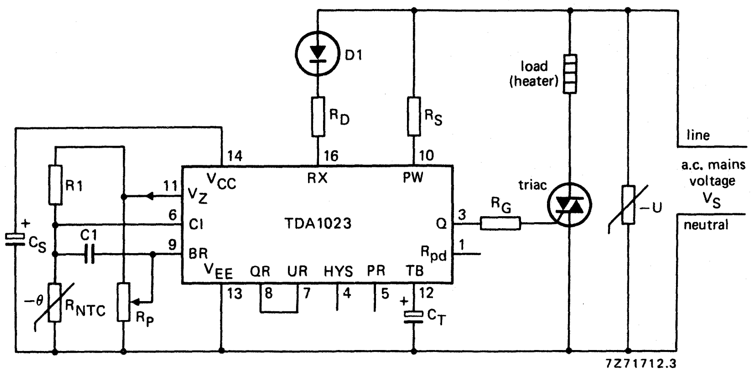

Fig. 15 The TDA1023 used in a 1200 to 2000 W heater with triac BT139. For component values see Table 3.

Conditions

Mains supply: V_S = 220 V

Temperature range = 5 to 30 °C

BT139 data: $V_{GT} < 1,5$ V; $I_{GT} > 70$ mA; $I_L < 60$ mA; at T_j = 25 °C

Table 3. Temperature controller component values (see Fig. 15).

parameter	symbol	value	remarks
Trigger pulse width	t_w	75 μs	see BT139 data sheet
Synchronization resistor	R_S	180 kΩ	see Fig. 13
Gate resistor	R_G	110 Ω	see Fig. 6
Max. average gate current	$I_{3(AV)}$	4,1 mA	see Fig. 8
Hysteresis resistor	R4	n.c.	see Table 1
Proportional band resistor	R5	n.c.	see Table 1
Min. required supply current	$I_{16(AV)}$	11,1 mA	
Mains dropping resistor	R_D	6,2 kΩ	see Fig. 10
Power dissipated in R_D	P_{RD}	4,6 W	see Fig. 10
Timing capacitor (eff. value)	C_T	68 μF	see Table 2
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 593 62512
Rectifier diode	D1	BYW56	
Resistor to pin 11	R1	18,7 kΩ	1% tolerance
NTC thermistor (at 25 ^oC)	R_{NTC}	22 kΩ	B = 4200 K cat. no. 2322 642 12223
Potentiometer	R_P	22 kΩ	
Capacitor between pins 6 and 9	C1	47 nF	
Smoothing capacitor	C_S	220 μF; 16 V	
If R_D and D1 are replaced by C_D and R_{SD}			
Mains dropping capacitor	C_D	470 nF	see Fig. 14
Series dropping resistor	R_{SD}	390 Ω	see Fig. 14
Power dissipated in R_{SD}	P_{RSD}	0,6 W	see Fig. 14
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 594 62512

Notes

1. ON/OFF control: pin 12 connected to pin 13.
2. If translation circuit is not required: slider of R_P to pin 7; pin 8 open; pin 9 connected to pin 11.

APPLICATION INFORMATION SUPPLIED ON REQUEST

CONTROL CIRCUIT FOR SWITCHED-MODE POWER SUPPLY

GENERAL DESCRIPTION

The TDA1060 is a bipolar integrated circuit intended for the control of a switched-mode power supply. It incorporates all the control functions likely to be required in switched-mode power supplies for professional equipment.

The circuit features:

- Suitability for a wide range of supply voltages
- Built-in stabilized power supply for external circuitry
- Built-in temperature-compensated voltage reference
- Adjustable frequency
- Adjustable control loop sensitivity
- Adjustable pulse width
- Adjustable maximum duty factor
- Adjustable overcurrent protection limit
- Low supply voltage protection with hysteresis
- Loop fault protection
- Slow-start facility
- Feed-forward facility
- Core saturation protection facility
- Overvoltage protection facility
- Remote ON/OFF switching facility

QUICK REFERENCE DATA

Supply voltage (voltage source)	V_{CC}	max.	18	V
Supply current (current source)	I_{CC}	max.	30	mA
Output current	$-I_{14}; I_{15}$	max.	40	mA
Stabilized voltage	V_Z	typ.	8,4	V
Reference voltage	V_{ref}	typ.	3,72	V
Output pulse repetition frequency range	f_o		50 Hz to 100	kHz
Operating ambient temperature range				
TDA1060; T	T_{amb}		−25 to + 125	°C
TDA1060A	T_{amb}		0 to + 70	°C
TDA1060B	T_{amb}		−55 to + 150	°C

PACKAGE OUTLINES

TDA1060, TDA1060A: 16-lead DIL; plastic (SOT-38).
TDA1060B: 16-lead DIL ceramic (cerdip) (SOT-74A, B, C).
TDA1060T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

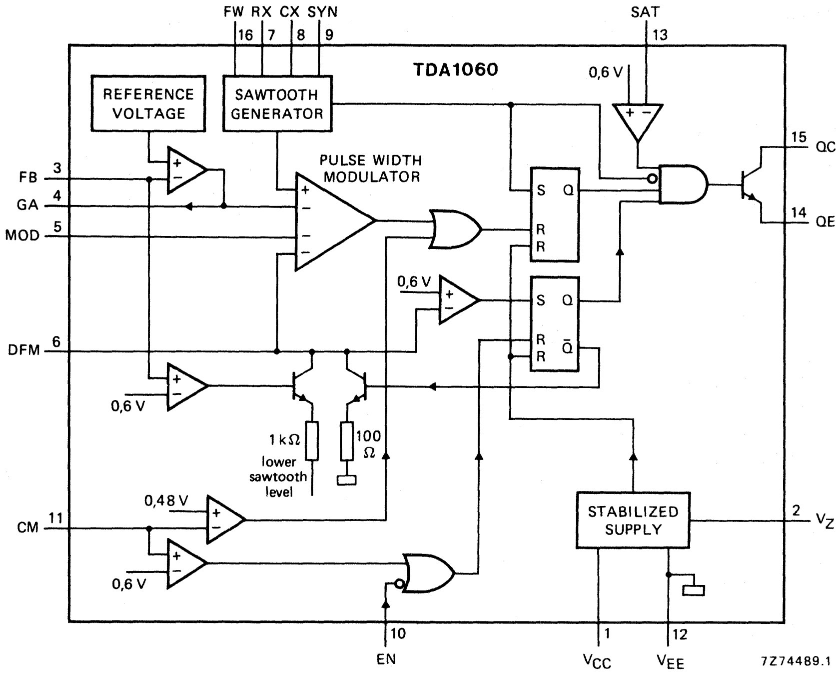

Fig. 1 Block diagram.

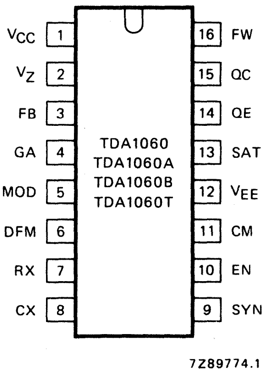

Fig. 2 Pinning diagram.

PINNING

1	V_{CC}	positive supply connection
2	V_Z	stabilized voltage output
3	FB	feedback input
4	GA	gain adjustment output
5	MOD	modulation input
6	DFM	maximum duty factor input
7	RX	external resistor connection
8	CX	external capacitor connection
9	SYN	synchronization input
10	EN	ENABLE input
11	CM	overcurrent protection input
12	V_{EE}	common
13	SAT	core saturation and overvoltage protection input
14	QE	emitter output
15	Q_C	collector output
16	FW	feed-forward input

FUNCTIONAL DESCRIPTION

The TDA1060 contains the control loop for a fixed-frequency pulse-duration regulated SMPS. The device works as follows. The output voltage V_O of the SMPS is sensed via a feedback network and compared with an internal reference voltage V_{ref}. Any difference between V_O and V_{ref} is amplified and fed to a pulse-width modulator (PWM), where it is compared with the instantaneous level of a ramp waveform (sawtooth) from an oscillator. The output from the PWM is a rectangular waveform synchronized with the oscillator waveform; its duty factor depends on the difference between V_O and V_{ref}. This signal drives the base of the SMPS power switching transistor so that its conduction period and hence the amount of energy transferred from the input to the output of the SMPS is controlled, resulting in a constant output voltage.

Stabilized power supply: V_{CC} and V_Z (pins 1 and 2)

The circuit contains a voltage/current regulator and may be supplied either by a current source (e.g. a series resistor connected to the high voltage input of the SMPS), or a voltage source (e.g. a 12 V battery).

The stabilized voltage, typically 8,4 V, is also available at V_Z, pin 2 for supplying external circuitry, e.g. a potentiometer to adjust the maximum duty factor. This supply output is protected against short-circuits. The current drawn from this output increases the total IC supply current by the same amount.

When the supply voltage V_{CC} becomes too low, i.e. $V_{CC} < V_Z + 0{,}2$ V, the circuit is automatically switched off. As soon as the supply voltage exceeds this threshold value by more than 0,2 V the circuit starts the SMPS via the slow start procedure.

Operating frequency: RX and CX (pins 7 and 8)

The frequency of the sawtooth generator, and hence of the output pulses, is set by an external resistor R7 at RX, pin 7, and an external capacitor C8 at CX, pin 8 (see Fig. 7). The frequency may be set between 50 Hz and 100 kHz and is virtually independent of the supply voltage.

Maximum duty factor and slow start: DFM (pin 6)

The maximum duty factor is set by the voltage on the duty factor input DFM (see Fig. 4). This voltage usually is derived from the stabilized power supply V_Z, pin 2, by an external voltage divider, see Fig. 8. As the upper and lower levels of the sawtooth waveform are set by an internal voltage divider, the accuracy of the maximum duty factor setting is determined by resistor ratios rather than by absolute values.

In case of a short-circuited feedback loop ($V_{3\text{-}12}$ less than typ. 600 mV) the duty factor input is internally biased to the lower level of the sawtooth waveform via a resistor of typ. 1 kΩ. The maximum duty factor permitted in that case sets a maximum limit to the impedance level of the external voltage divider at pin 6.

During the flyback of the sawtooth the output pulse is inhibited. For a 1 nF capacitor C8 at pin 8 this flyback time is 1 μs. This sets a natural limit to the duty factor.

The time constant for the slow start is determined by an external capacitor connected between the maximum duty factor input DFM and V_{EE}, pin 12, together with the impedance of the voltage divider at pin 6. This capacitor also determines the dead time before the slow start procedure for remote ON/OFF or when the current sensing voltage has exceeded 600 mV, see below.

If the DFM input is note used it should be connected to V_Z via a resistor of 5 kΩ.

FUNCTIONAL DESCRIPTION (continued)

Control loop sensitivity, stability, and feedback loop fault protection, FB and GA (pins 3 and 4)

The device contains a control loop error amplifier, i.e. a differential amplifier that compares the voltage on the feedback input FB, pin 3, with the internal reference voltage. This reference voltage is a temperature-compensated voltage source based on the band-gap energy of silicon.

The control loop sensitivity is determined by the closed-loop gain A_f of the error amplifier. Normally the output from the SMPS is connected to the feedback input FB via a voltage divider and a series resistor. The closed-loop gain of the error amplifier is set by applying feedback from the gain adjustment output GA, pin 4, to the feedback input FB by a resistor R3-4, see Fig. 8.

To avoid instability a capacitor should be connected between the gain output GA and V_{EE}, pin 12. A 22 nF capacitor will cause the frequency response to fall off above 600 Hz.

The feedback input FB is internally biased to the HIGH level, this gives a protection against a feedback loop fault: an open feedback loop will make the duty factor zero.

A shorted feedback loop (feedback voltage less than typ. 600 mV) causes the maximum duty factor input DFM to be internally biased to the lower level of the sawtooth waveform via a resistor of typ. 1 kΩ, thus substantially reducing the maximum duty factor. This duty factor will then be determined by the impedance of the external voltage divider at DFM, pin 6, and the internal biasing resistor.

Overcurrent protection input CM (pin 11)

There are two current limits, corresponding with voltages on the overcurrent protection input CM of typ. 480 mV and 600 mV. As soon as the voltage on this input exceeds 480 mV, the running output pulse is immediately terminated; the next pulse starts normally at the next period. If the voltage exceeds 600 mV, the output pulses are inhibited for a certain dead time, during which the slow start capacitor at pin 6 is unloaded. After this the circuit starts again with the slow start procedure.

If the overcurrent protection input CM is not used, it should be connected to V_{EE}, pin 12.

Feed-forward input FW (pin 16)

The feed-forward input FW can be connected to an external voltage divider from the input voltage of the SMPS, see Fig. 8. It has the effect of varying the supply voltage of the sawtooth generator with respect to the stabilized voltage. When the voltage on the feed-forward input increases, the upper level of the sawtooth is also increased. Since neither the voltage level that sets the maximum duty factor nor the feedback voltage are influenced by the feed-forward, the duty factor reduces (see Fig. 6). This can therefore compensate for mains voltage variations.

If feed-forward is not required the feed-forward input FW should be connected to V_{EE}, pin 12.

Synchronization input SYN (pin 9)

The frequency of the sawtooth waveform, and hence of the output pulses, can be synchronized via the TTL compatible synchronization input SYN. The synchronizing frequency must be lower than the oscillator free-running frequency. When the synchronization input is LOW the sawtooth generator is stopped; it starts again when the input goes HIGH. Synchronization pulses do not influence the slope of the sawtooth, and hence not the width of the output pulses, they only change their separation in time.

For free-running operation it is advisable to connect the synchronization input SYN to V_Z, pin 2.

Core saturation and overvoltage protection input SAT (pin 13)

To obtain a protection against core saturation, especially during transient conditions, the output transformer of the SMPS has to be fitted with a winding serving as a current sensor. Its output voltage is rectified and fed to the SAT input.

This core saturation protection may be combined with an overvoltage protection. To this end a portion of the SMPS output voltage is also fed to the SAT input either via a voltage divider or via a suitable regulator diode (zener diode). The output pulses are inhibited as long as the voltage on this input exceeds the threshold voltage, typ. 600 mV.

The voltage at the SAT input does not influence the frequency of the sawtooth generator and hence not of the output pulses.

If none of these protection facilities are used, the SAT input should be connected to V_{EE}, pin 12.

Remote ON/OFF switching: ENABLE input EN (pin 10)

The output pulses can be switched on and off by applying logic levels to the TTL compatible ENABLE input. A LOW level causes immediate inhibition of the output pulses, a subsequent HIGH level switches the circuit on with the slow-start procedure.

If this facility is not required, EN should be connected to V_Z, pin 2.

Modulation input MOD (pin 5)

The duty factor of the output pulses may be reduced below the value resulting from the voltages on the maximum duty factor input DFM and the gain adjust output GA by applying a lower voltage to the modulation input MOD. This input may be used with an external control loop, e.g. for constant-current control, or to obtain a fold-back characteristic.

If the modulation input is not used, it should be connected to V_Z, pin 2.

Output QC and QE (pins 13 and 14)

To avoid double pulses that might occur at an excessively low mains voltage or an excessively high output current the output is preceded by a latch. The two outputs offer a choice of output current polarity, QC giving a positive current, i.e. a current flowing into the output, and QE giving a negative current, a current flowing out of the output. The two connections have the additional advantage that the relatively large output currents do not flow through the V_{CC} and V_{EE} connections, where they could induce noise.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (voltage source)	V_{CC}	−0,5 to + 18 V
Supply current (current source)	I_{CC}	max. 30 mA
Feed-forward input voltage range		
$V_{CC} < 24$ V	$V_{16\text{-}12}$	0 to V_{CC} V
$V_{CC} > 24$ V	$V_{16\text{-}12}$	0 to 24 V
Input voltage range (all other inputs)	V_I	0 to V_Z V
Emitter output voltage range	$V_{14\text{-}12}$	0 to 5 V
Collector output voltage range	$V_{15\text{-}12}$	0 to V_{CC} V
Output current		
d.c. (see Figs 3a, c and e)	$-I_{14}; I_{15}$	max. 40 mA
peak; t = max. 1 μs; duty factor d < 10%	$-I_{14}; I_{15}$	max. 200 mA
Storage temperature range		
→ TDA1060; T	T_{stg}	−55 to + 150 °C
→ TDA1060A	T_{stg}	−55 to + 150 °C
→ TDA1060B	T_{stg}	−55 to + 150 °C
Operating ambient temperature range		
TDA1060; T	T_{amb}	−25 to + 125 °C
TDA1060A	T_{amb}	0 to + 70 °C
TDA1060B	T_{amb}	−55 to + 150 °C
Power dissipation (see Figs 3b, d and f)	P_{tot}	max. 1 W

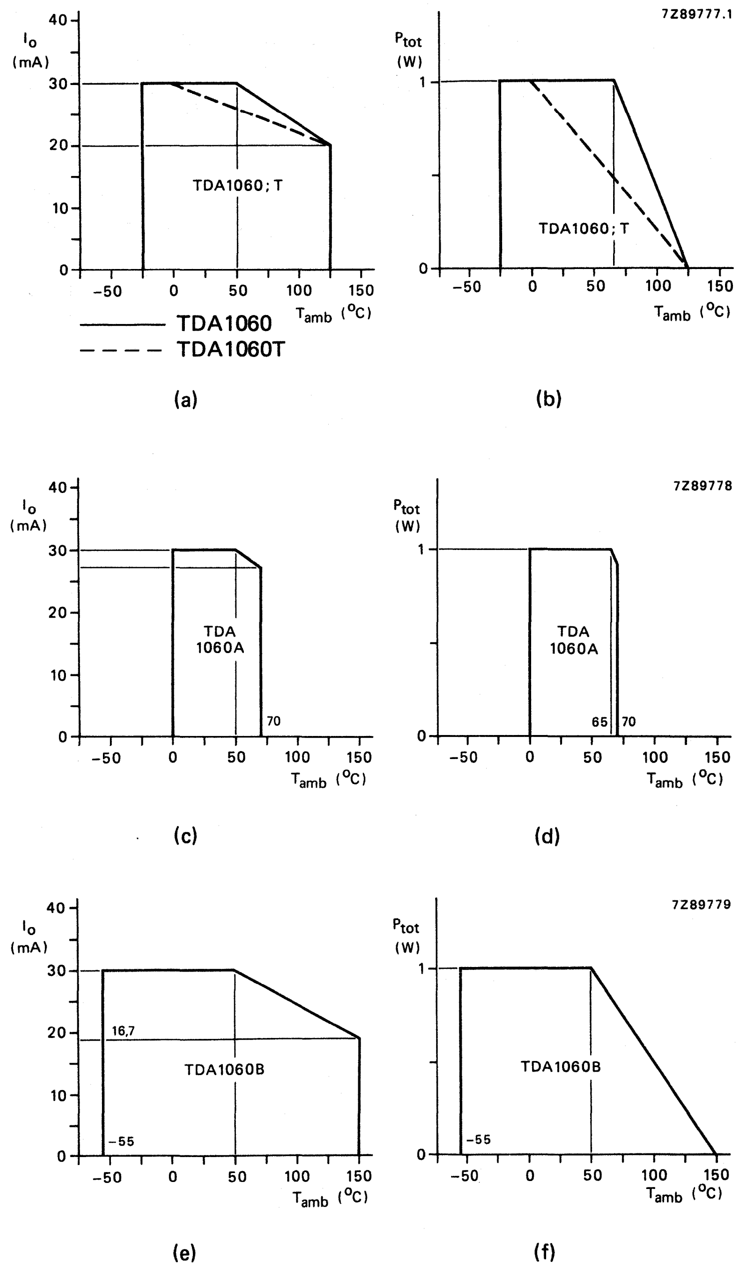

Fig. 3 Output current and power dissipation derating curves.

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = operating ambient temperature range, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Operating ambient temperature range					
TDA1060; T	T_{amb}	−25	–	125	°C
TDA1060A	T_{amb}	0	–	70	°C
TDA1060B	T_{amb}	−55	–	150	°C
Supply V_{CC} (pin 1)					
Supply voltage at I_{CC} = 15 mA TDA1060; T	V_{CC}	18,5	23	27	V
TDA1060A	V_{CC}	18,5	23	27	V
TDA1060B	V_{CC}	18	23	27,5	V
at I_{CC} = 30 mA TDA1060; T	V_{CC}	19,5	24	29	V
TDA1060A	V_{CC}	19,5	24	29	V
TDA1060B	V_{CC}	19	24	29,5	V
Supply current; R7 = 25 kΩ; duty factor δ = 50%; I_Z = 0; at T_{amb} = 25 °C	I_{CC}	2,5	–	10	mA
over ambient temperature range	I_{CC}	2,5	–	15	mA
Threshold voltage of low supply voltage protection at T_{amb} = 25 °C	V_{CC}	8,85	–	10,8	V
Variation with temperature	$-\Delta V_{CC}/\Delta T$	–	7,5	–	mV/K
Hysteresis of low supply voltage protection	ΔV_{CC}	–	500	–	mV
Stabilized supply output V_Z (pin 2)					
Output voltage at T_{amb} = 25 °C	V_Z	7,5	8,4	9	V
Variation with temperature	$\Delta V_Z/\Delta T$	−1,5	–	+ 1,5	mV/K
Output current	$-I_Z$	–	–	5	mA
Feedback input FB (pin 3)					
Input voltage, feedback operation	$V_{3\text{-}12}$	2	–	V_Z-1	V
Input current at $V_{3\text{-}12}$ = 2 V	$-I_3$	1,5	12	35	µA
Internal reference voltage, measured at pin 3; pins 3 and 4 interconnected and grounded via a 100 nF capacitor; T_{amb} = 25 °C	V_{ref}	3,42	3,72	4,03	V
Variation with temperature	$\frac{\Delta V_{ref}/V_{ref}}{\Delta T}$	–	0,01	–	%/K
Variation with supply voltage	$\frac{\Delta V_{ref}}{\Delta V_{CC}}$	–	0,8	–	mV/V

parameter	symbol	min.	typ.	max.	unit
Long-term variation with time	$\pm \Delta V_{ref}/\Delta t$	–	2	–	μV/h
Threshold voltage of feedback loop short-circuit protection at $T_{amb} = 25\,^{o}C$	$V_{3\text{-}12}$	470	600	720	mV
Variation with temperature	$\frac{\Delta V_{3\text{-}12}/V_{3\text{-}12}}{\Delta T}$	–	0,01	–	%/K
Gain adjustment output GA (pin 4)					
Open-loop gain, pin 3 to pin 4	A_o	–	60	–	dB
External feedback resistance	$R_{3\text{-}4}$	10	–	–	kΩ
Modulator input MOD (pin 5)					
Input current at $V_{5\text{-}12} = 2$ V; $V_{4;\,6\text{-}12} > 2$ V	$-I_5$	–	–	5	μA
Maximum duty factor input DFM (pin 6)					
Input voltage for limiting the duty factor to 50%; $f_o = 20$ to 50 kHz; $V_{16\text{-}12} = 0$ V	$V_{6\text{-}12}$	–	$0{,}42V_Z$	–	V
Input current at $V_{6\text{-}12} = 2$ V	$-I_6$	–	–	6	μA
Capacitor discharge current during fault condition	I_6	2,5	–	–	mA
Minimum output OFF time at C7 = 1,8 nF	t_{off}	–	1	–	μs
Variation of max. duty factor with temperature at $f_o = 20$ kHz and $\delta_{max} = 50\%$	$\Delta\delta_{max}/\Delta T$	–	0,02	–	%/K
Internal biasing resistor to V_{EE} at $V_{3\text{-}12} = 0$ V	$R_{6\text{-}12}$	0,75	1	1,25	kΩ
Synchronization input SYN (pin 9)					
Input voltage, sawtooth ON	V_{IH}	2	–	V_Z	V
sawtooth OFF: TDA1060; TDA1060A; TDA1060T	V_{IL}	0	–	0,8	V
TDA1060B	V_{IL}	0	–	0,6	V
Input current at $V_{9\text{-}12} = 0$ V	$-I_{IL}$	20	–	120	μA
External resistor connection RX (pin 7)					
External frequency adjustment resistor	R7	5	–	40	kΩ
External capacitor connection CX (pin 8)					
Sawtooth, upper level at $V_{16\text{-}12} = 0$ V	$V_{8\text{-}12}$	–	5,7	–	V
lower level	$V_{8\text{-}12}$	–	1,3	–	V
Oscillator frequency R7 = 6,4 kΩ, C8 = 6,4 nF	f_{osc}	–	30,5	–	kHz
Output pulse repetition frequency range	f_o	0,05	–	100	kHz
Variation with temperature	$\frac{\Delta f_o/f_o}{\Delta T}$	–	0,03	–	%/K

7

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Feed-forward input FW (pin 16)					
Input voltage					
for $V_{CC} < 24$ V	$V_{16\text{-}12}$	0	–	V_{CC}	V
for $V_{CC} > 24$ V	$V_{16\text{-}12}$	0	–	24	V
Input current at $V_{16\text{-}12}$ = 16 V; V_{CC} = 18 V; T_{amb} = 25 °C	I_{16}	–	–	5	μA
Frequency variation with input voltage at $V_{16\text{-}12} > 8$ V	$\frac{\Delta f_o/f_o}{\Delta V_{16\text{-}12}}$	–	1	–	%/V
Overcurrent protection input CM (pin 11)					
Input voltage	$V_{11\text{-}12}$	0	–	V_Z	V
Input threshold voltage for single pulse inhibit (current limit mode); T_{amb} = 25 °C	V_{T1}	400	–	500	mV
Ratio of threshold voltages for shot down/ slow start and for single pulse inhibit	V_{T2}/V_{T1}	–	1,25	–	
Threshold variation with temperature	$\Delta V/\Delta T$	–	125	–	μV/K
Input current at $V_{11\text{-}12}$ = 250 mV	$-I_{11}$	–	–	10	μA
Turn-off delay, I_{15} = 40 mA; $V_{11\text{-}12} = 1{,}2 \times V_{T1}$	t_d	–	–	1,0	μs
Core saturation and overvoltage protection input SAT (pin 13)					
Input voltage	$V_{13\text{-}12}$	0	–	V_Z	V
Input threshold voltage at T_{amb} = 25 °C	$V_{13\text{-}12}$	470	600	720	mV
Threshold variation with temperature	$\Delta V/\Delta T$	–	125	–	μV/K
Input current at $V_{13\text{-}12}$ = 250 mV	$-I_{13}$	–	–	7	μA
ENABLE input EN (pin 10)					
Input voltage					
ON	V_{IN}	2	–	V_Z	V
OFF: TDA1060; TDA1060A; TDA1060T	V_{IL}	0	–	0,8	V
TDA1060B	V_{IL}	0	–	0,6	V
Input current at $V_{10\text{-}12}$ = 0 V	$-I_{IL}$	20	–	120	μA
Outputs QC and QE (pins 14 and 15)					
Output current	$-I_{14}; I_{15}$	40	–	–	mA
Emitter output voltage	$V_{14\text{-}12}$	–	–	5	V
Collector output voltage at $V_{14\text{-}12}$ = 0 V; I_{15} = 40 mA	$V_{15\text{-}14}$	–	–	500	mV

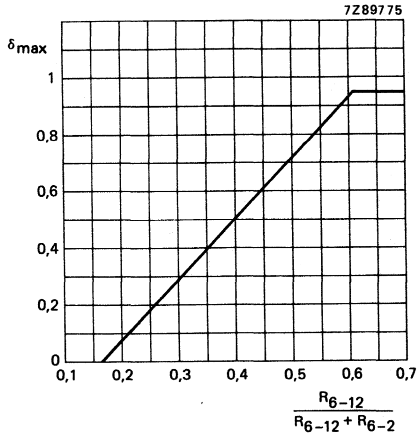

Fig. 4 Maximum duty factor δ_{max} as a function of the voltage divider ratio at the duty factor input DFM.

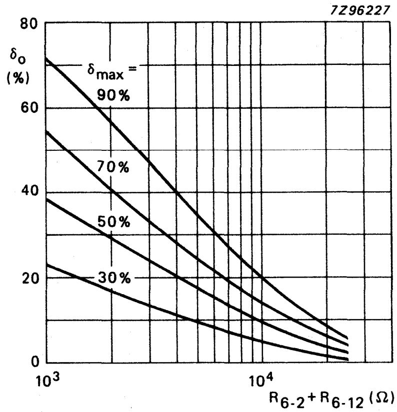

Fig. 5 Soft-start minimum duty factor (δ_o) as a function of $R_{6\text{-}2}$ and $R_{6\text{-}12}$.

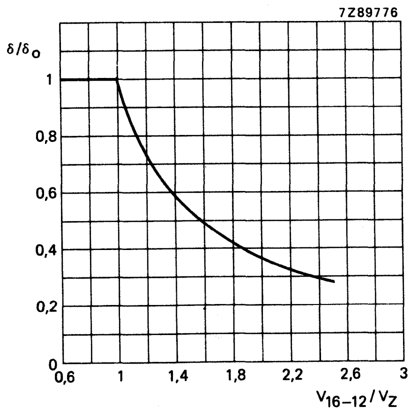

Fig. 6 Feed-forward regulation characteristic. Duty factor δ as a function of the voltage $V_{16\text{-}12}$ on the feed-forward input FW. δ_o is the duty factor for $V_{16\text{-}12} \leqslant V_Z$.

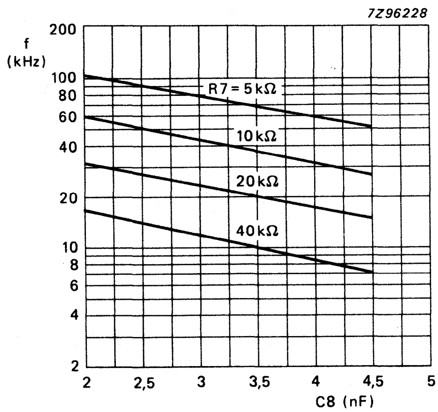

Fig. 7 Typical frequency as a function of C8 (R7 as parameter).

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APPLICATION INFORMATION

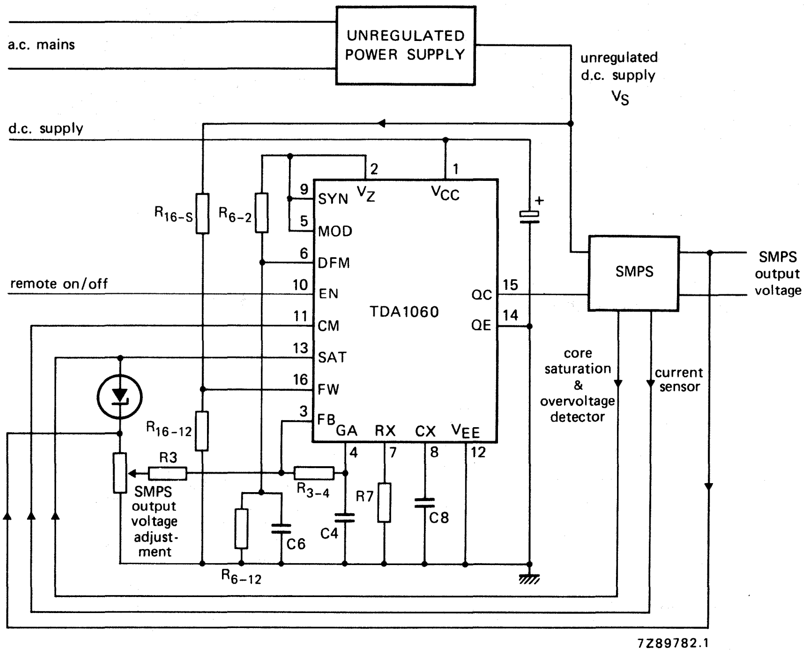

Fig. 8 Connections to the TDA1060 in a switched-mode power supply.

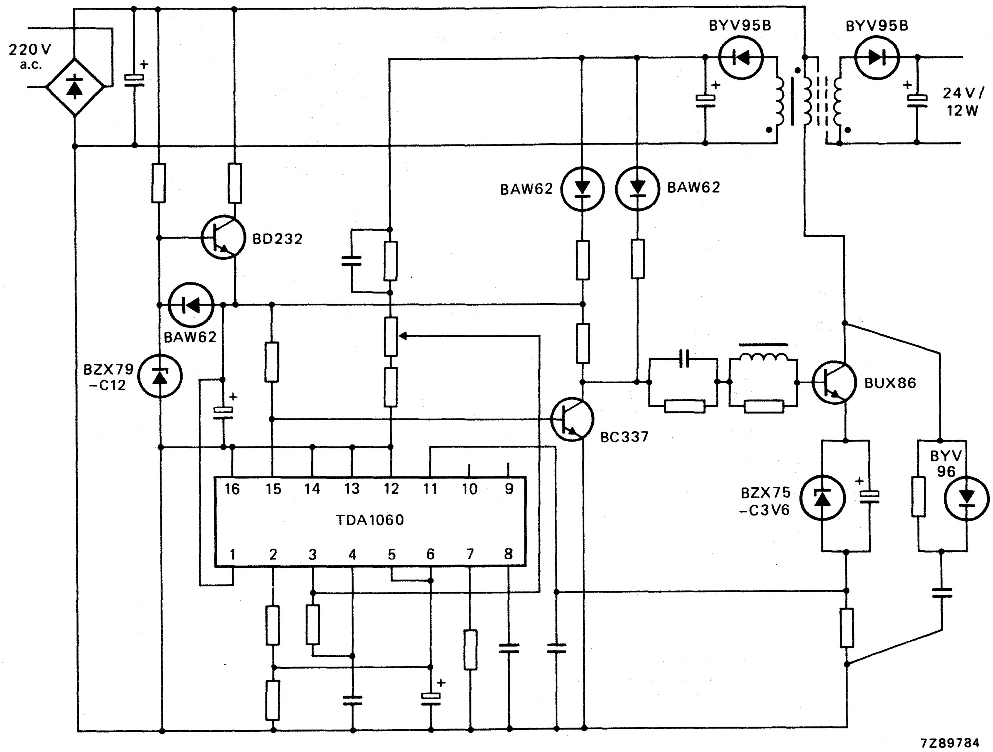

Fig. 9 Application of the TDA1060 in a 24 V, 12 W SMPS with flyback converter.

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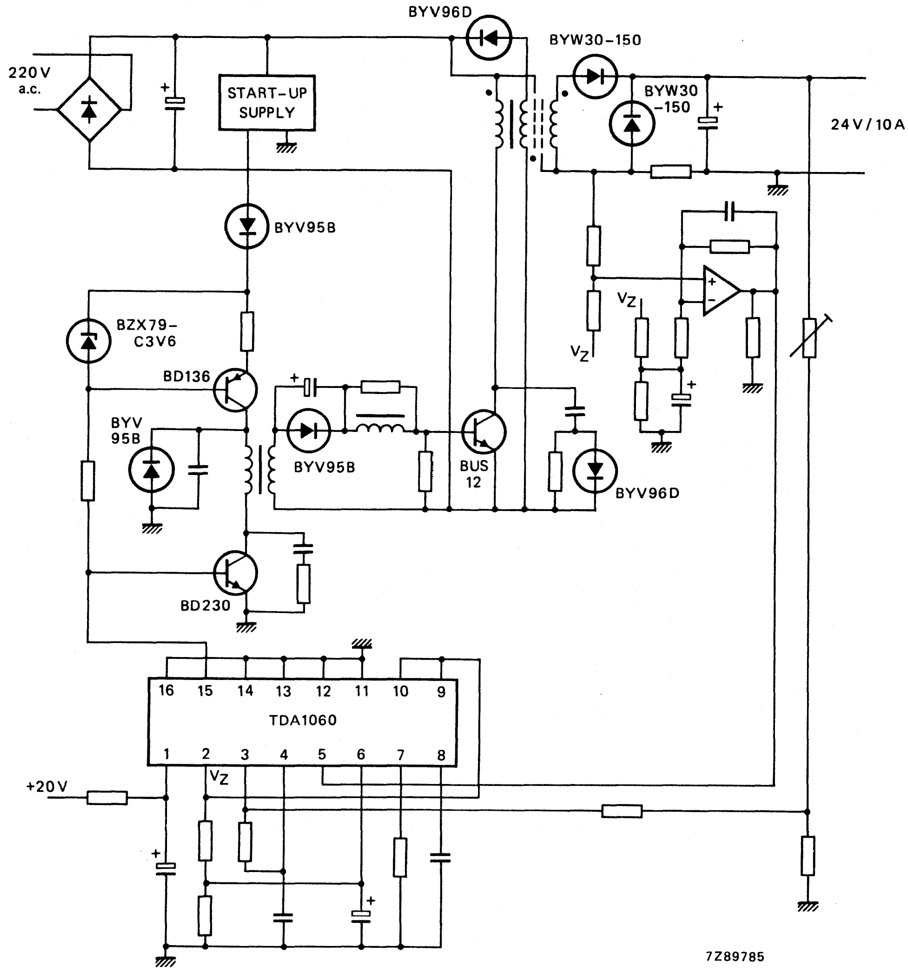

Fig. 10 Application of the TDA1060 in a 24 V, 240 W SMPS with forward converter.

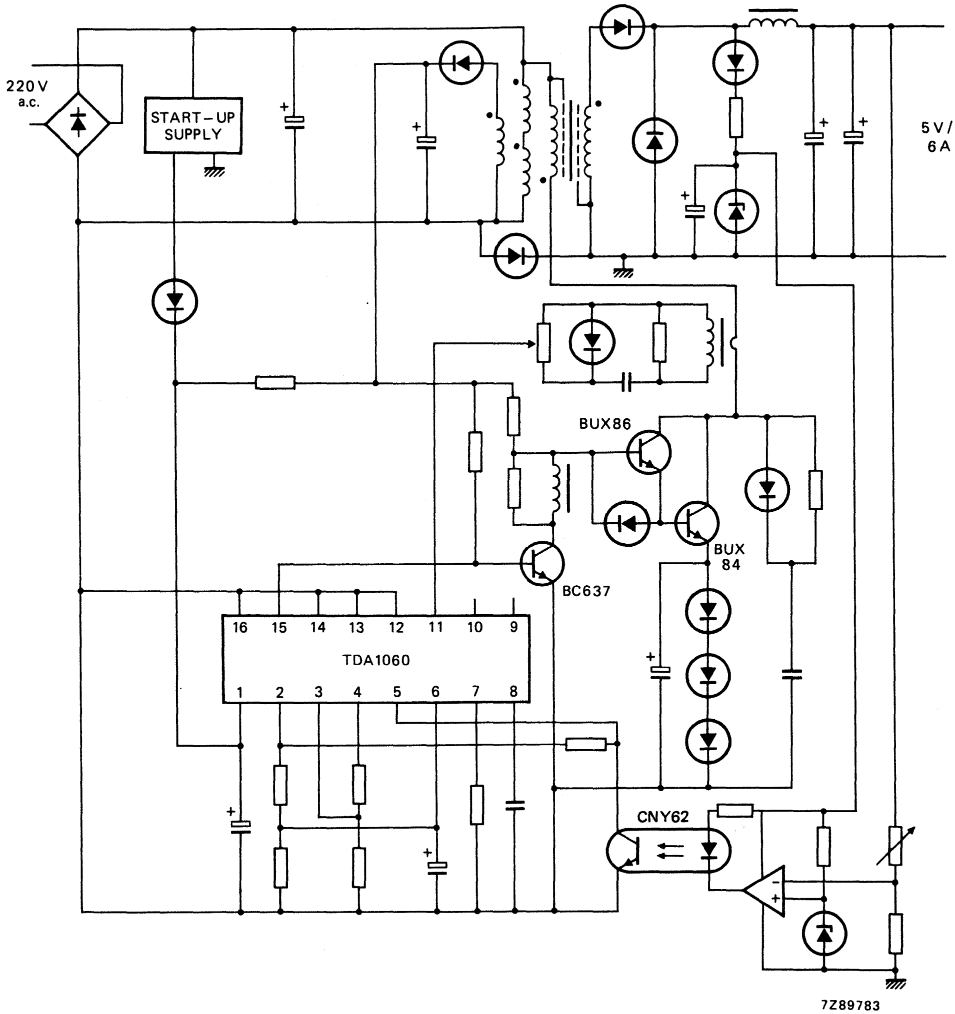

Fig. 11 Application of the TDA1060 in a 5 V, 30 W SMPS with forward converter and with an optocoupler CNY62 for voltage separation.

APPLICATION INFORMATION SUPPLIED UPON REQUEST.

I.F. LIMITING AMPLIFIER, FM DETECTOR & AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDB1080 is a bipolar integrated circuit comprising a limiting amplifier, a balanced FM detector and a class-B audio amplifier. It is intended for frequencies up to 500 kHz with either narrow-band or wide-band FM. The circuit is especially suited for use in portophone sets, where a low supply voltage, a low supply current and a high sensitivity are of paramount importance.

QUICK REFERENCE DATA

Supply voltage range				
I.F. part	V_{CC1}		2,3 to 3,5	V
A.F. part	V_{CC2}		2,3 to 10	V
Supply current at $V_{CC1} = V_{CC2} = 2,5$ V, no signal	$I_{CC1} + I_{CC2}$	typ.	3	mA
Input voltage at onset of limiting	$V_{I1lim(rms)}$	typ.	30	μV
AM rejection at $V_i = 1$ mV	k_{AMR}	typ.	50	dB
Open-loop voltage amplification of audio amplifier	A_{vd}	typ.	200	
Output power of audio amplifier at $V_{CC2} = 9$ V	P_o	typ.	65	mW
Operating ambient temperature range	T_{amb}		−20 to + 70	^oC

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PACKAGE OUTLINES

TDB1080: 16-lead DIL; plastic (SOT-38WE-2).

TDB1080T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

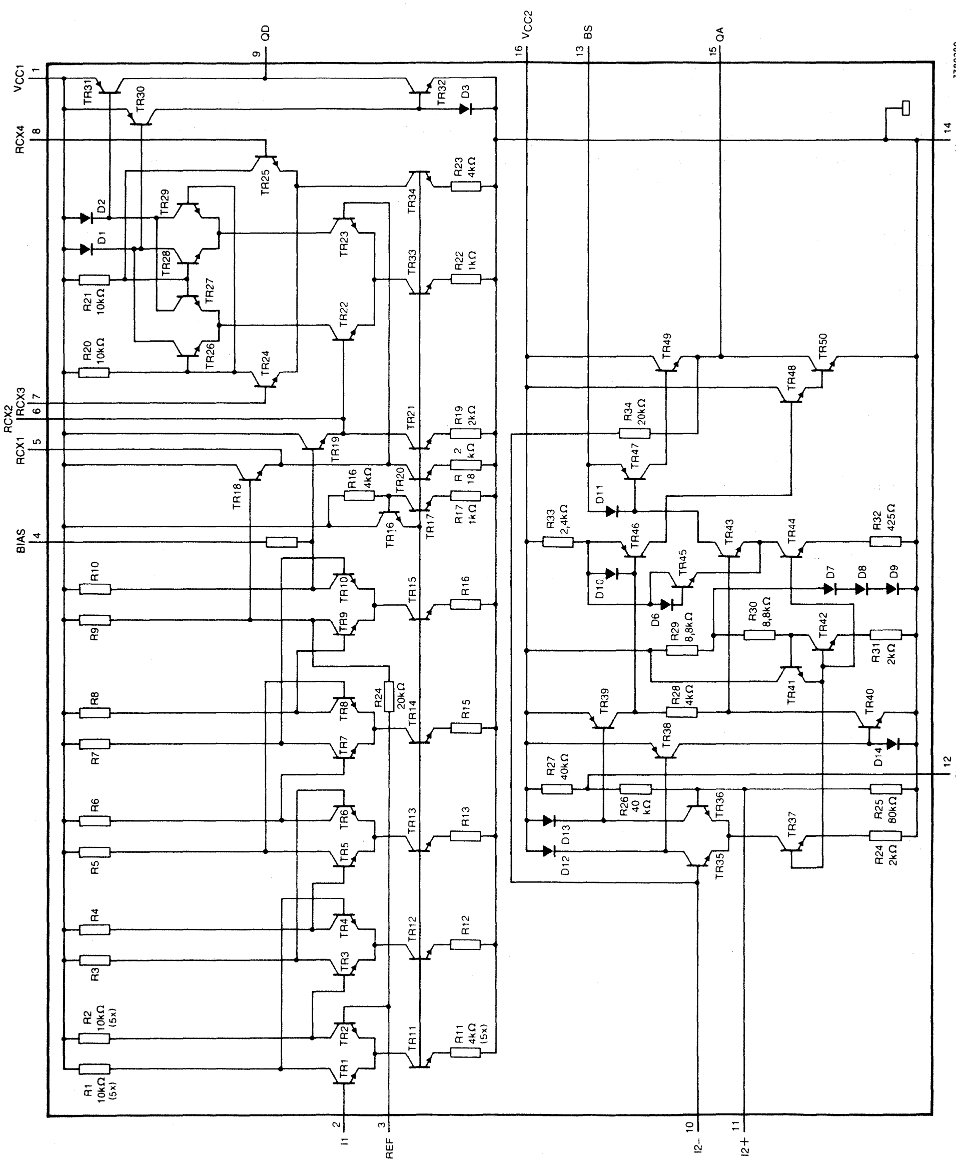


Fig. 1 Circuit diagram.

PINNING

1	V_{CC1}	positive supply, limiting amplifier
2	I1	limiting amplifier input
3	REF	reference input, limiting amplifier
4	BIAS	input biasing output
5	RCX1	external RC network
6	RCX2	external RC network
7	RCX3	external RC network
8	RCX4	external RC network
9	QD	FM detector output
10	I2–	out-of-phase input, audio amplifier
11	I2+	in-phase input, audio amplifier
12	CX	external capacitor
13	BS	bootstrap
14	V_{EE}	ground
15	QA	audio amplifier output
16	V_{CC2}	positive supply, audio amplifier

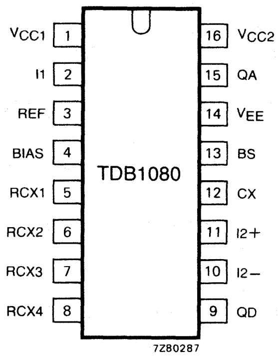


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TDB1080 consists of two parts that may be used independently, viz. a limiting i.f. amplifier with balanced FM detector, and a class-B audio amplifier.

Supply

The two parts of the circuit have a common-ground pin V_{EE} but separate supply pins V_{CC1} and V_{CC2}. The limiting amplifier and detector may be used with a supply voltage up to 3,5 V, the audio amplifier up to 10 V. The circuit is built to a large extent on the basis of long-tailed pairs with current sources in their tails. Thanks to the stabilizer diodes (D7, D8 and D9) the supply current of the audio amplifier varies little with the supply voltage. This permits the circuit to be used over a wide supply voltage range without an excessive battery drain as a result.

Limiting amplifier inputs I1 and REF and biasing output BIAS (pins 2, 3 and 4)

The limiting amplifier has differential inputs I1 and REF. I1 is intended to be used as an input; it should be biased externally by connecting it to the input biasing output BIAS via a resistor or an inductor. The reference input REF is biased internally; it should be decoupled by connecting a capacitor from REF to ground.

The onset of limiting is specified as the input voltage giving 3 dB gain reduction.

External RC network pins RCX1 to RCX4 (pins 4 to 8)

The TDB1080 contains a quadrature detector which requires an RC phase shifting network. This has to be connected to RCX1, RCX2, RCX3 and RCX4 as shown in Fig. 4. The component values have to be chosen in accordance with the i.f. centre frequency.

Audio amplifier inputs I2+ and I2– (pins 11 and 10)

The audio amplifier has differential inputs I2+ and I2– which are biased internally.

FUNCTIONAL DESCRIPTION (continued)

External capacitor pin CX (pin 12)

The internal biasing network for input I2+ should be decoupled by connecting an external capacitor between CX and ground.

Audio amplifier output QA and bootstrap pin BS (pins 15 and 13)

The audio amplifier has a class-B output stage. The maximum output voltage swing is obtained by connecting a capacitor between the bootstrap pin BS and the output QA and the load from BS to V_{CC2} (see Fig. 4).

The maximum output power varies from typ. 15 mW at V_{CC2} = 2,5 V to typ. 65 mW at V_{CC2} = 9 V.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages, d.c.	V_{CC1}	max.	5 V
	V_{CC2}	max.	10 V
Supply current	$I_{CC1} + I_{CC2}$	max.	50 mA
Total power dissipation	P_{tot}	see Fig. 3	
Storage temperature range	T_{stg}	−55 to + 125 °C	
Operating ambient temperature range	T_{amb}	−20 to + 70 °C	

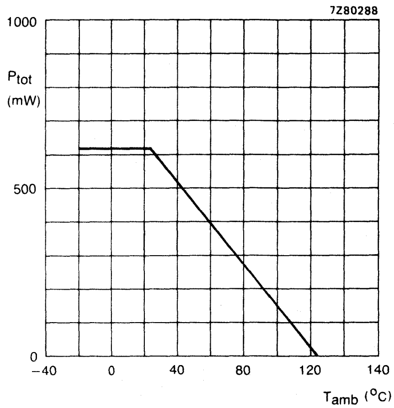


Fig. 3 Power derating curve.

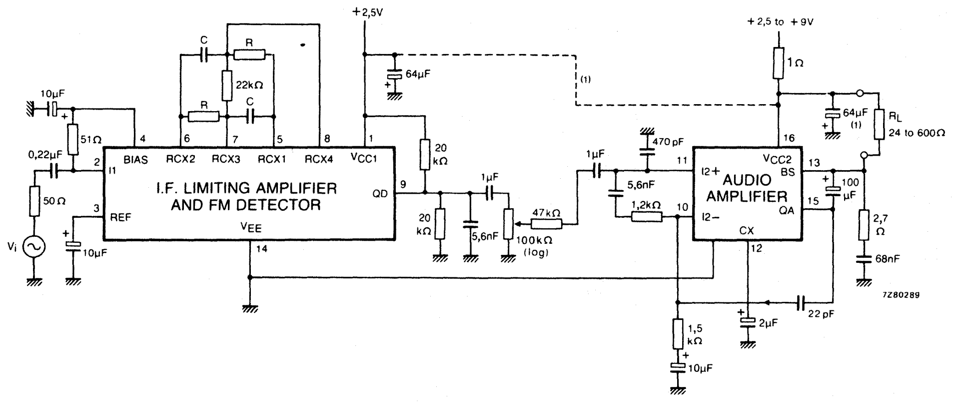
CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2,5$ V; $f_i = 95$ kHz; $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $T_{amb} = 25$ °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies V_{CC1} and V_{CC2} (pins 1 and 16)					
Supply voltages	V_{CC1}	2,3	2,5	3,5	V
	V_{CC2}	2,3	2,5	10	V
Supply currents					
at $V_{CC1} = 2,5$ V	I_{CC1}	–	1,5	2	mA
at $V_{CC2} = 2,5$ V, no signal	I_{CC2}	–	1,5	2	mA
at $V_{CC2} = 9$ V, no signal	I_{CC2}	–	3,5	–	mA
Limiting amplifier input I1 (pin 2)					
Input impedance	$\|z_{id}\|$	15	–	–	kΩ
Input voltage for onset of limiting (3 dB gain reduction)	$V_{I1lim(rms)}$	–	30	–	μV
Source impedance (between I1 and REF)	$\|Z_S\|$	–	–	5	kΩ
A.M. suppression at $\Delta f_i = 70$ Hz; $f_m = 1$ kHz; m = 0,3;					
$R_S = 50\ \Omega$					
at $V_{I1(rms)} = 300\ \mu$V	k_{AMR}	–	40	–	dB
at $V_{I1(rms)} = 1$ mV	k_{AMR}	–	50	–	dB
at $V_{I1(rms)} = 10$ mV	k_{AMR}	–	50	–	dB
$R_S = 5$ kΩ					
at $V_{I1(rms)} = 300\ \mu$V	k_{AMR}	–	30	–	dB
at $V_{I1(rms)} = 1$ mV	k_{AMR}	–	40	–	dB
at $V_{I1(rms)} = 10$ mV	k_{AMR}	–	50	–	dB
FM Detector output QD (pin 9)					
Output voltage at $d_{tot} = 0,5\%$;					
at $f_i = 95$ kHz; $\Delta f = \pm 50$ kHz	$V_{QD(rms)}$	100	–	–	mV
at $f_i = 250$ kHz; $\Delta f = \pm 50$ kHz	$V_{QD(rms)}$	100	–	–	mV
Signal-to-noise ratio					
at $f_i = 95$ kHz; $\Delta f = \pm 50$ kHz	S/N	70	–	–	dB
at $f_i = 250$ kHz; $\Delta f = \pm 50$ kHz	S/N	70	–	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Audio amplifier					
Open-loop voltage amplification	A_{vd}	–	200	–	
variation with frequency, f = 50 Hz to 15 kHz	ΔA_{vd}	−1,5	–	+ 1,5	dB
Load resistance	R_L	24	–	600	Ω
Output voltage at R_L = 24 Ω; d_{tot} = 1%	$V_{QA(rms)}$	–	600	–	mV
Total distortion at R_L = 24 Ω; $V_{QA(rms)}$ = 500 mV	d_{tot}	–	0,5	1	%
Output power at V_{CC2} = 9 V; R_L = 115 Ω; d_{tot} = 5%	P_{QA}	–	65	–	mW
Signal-to-noise ratio at R_L = 115 Ω; V_o = 600 mV; f = 0,5 to 11 kHz; 80 dB/octave cut-off filter	S/N	70	–	–	dB



(1) If V_{CC2} is equal to V_{CC1} pin 16 can be connected to pin 1 and the capacitor to pin 16 can be omitted.

Fig. 4 Test circuit and typical application of the TDB1080. For f_i = 95 kHz R = 100 kΩ and C = 82 pF, for f_i = 250 kHz R = 33 kΩ and C = 47 pF.

13-BIT SERIES-PARALLEL CONVERTER

GENERAL DESCRIPTION

The TEA1017 is a bipolar integrated circuit intended to drive displays, triacs and relays and small stepper motors. The data is serially shifted into the device and is stored in 13 latches that drive the outputs.

Features

- TTL and CMOS compatible inputs
- Outputs drive load in both directions
- Power-on reset makes outputs floating
- Wide supply voltage range

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4,5 to 18	V
Output current, each output	$I_{OL}; -I_{OH}$	max.	80	mA
Clock frequency	f_{CLK}	max.	50	kHz
Operating ambient temperature range	T_{amb}		0 to +80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS, HE, KE, ME)

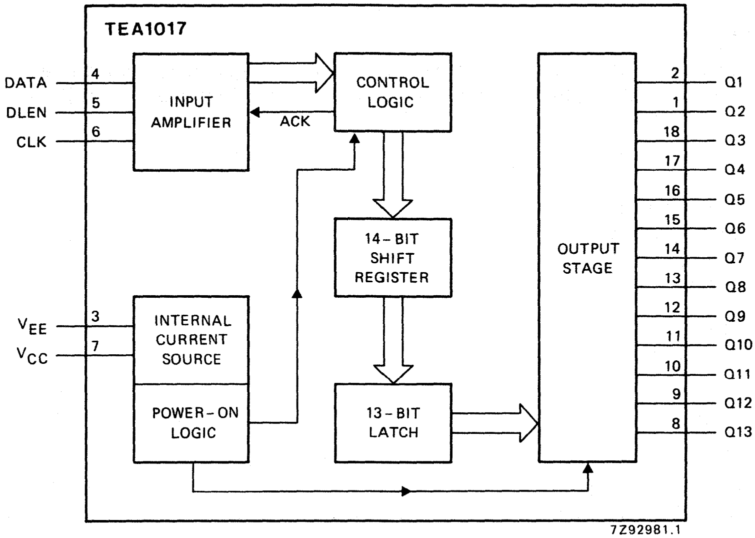


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The control logic performs a key function in this device. It checks whether the input information has the correct format: a DLEN signal that has been HIGH during 14 clock pulses, and a DATA signal with its first bit LOW.
When the format is found to be correct, the 15th clock pulse makes the control logic generate a signal that loads the content of the first 13 bits of the shift register into 13 latches. These drive the output stages.

"Acknowledge" (pin 4)

After the 15th clock pulse an acknowledge signal drives the DATA pin to LOW. To use this information the DATA should be programmed HIGH and an open collector-device, or a series resistor should be used on the DATA-input. This signal is valid till the next clock pulse, LOW-to-HIGH transition, see Fig. 3.

Supply V_{CC} (pin 7)

The supply current of the TEA1017 is regulated internally. This permits the circuit to be used over a very wide range of supply voltages, viz. 4,5 to 18 V, with little variation of supply current.

The circuit has a power-on reset arrangement that resets the circuit and sets the outputs to a high-impedance state. It requires a rise-time of the supply larger than 3 us/V.

DATA input (pin 4)

The circuit requires input information on the DATA input consisting of 14 bits, the first bit being LOW. This information should be synchronous with the clock pulse.
Data is loaded into the shift register at HIGH-to-LOW transitions of the clock pulse.

Data line enable input DLEN (pin 5)

A HIGH level on the DLEN input enables the shift register. This HIGH level should have a duration of 14 clock pulses (see Fig. 3).
After the DLEN input has returned to LOW the subsequent (15th) clock pulse transfers the contents of the shift register to the latches and then to the outputs.

Clock input CLK (pin 6)

The shift register shifts at the HIGH-to-LOW transitions of the clock pulse. The clock signal may be a continuously running clock or a clock burst of 15 clock pulses.

Outputs Q1 to Q13

The outputs are capable of supplying a load current in both directions, i.e. they can drive a load to the supply (V_{CC}) or to ground (V_{EE}).

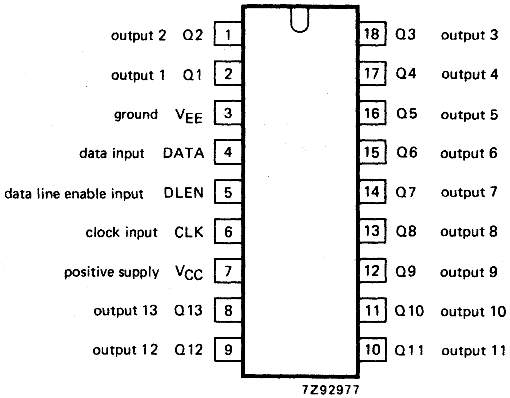


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	18	V
Input voltage range, all inputs	V_I		–0,3 to V_{CC} +0,3	V
Output current, all outputs				
HIGH	$-I_{OH}$	max.	150	mA
LOW	I_{OL}	max.	150	mA
Total power dissipation *	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		–40 to +150	°C
Operating ambient temperature range	T_{amb}		0 to + 80	°C

* See derating curve Fig. 4.

CHARACTERISTICS

V_{CC} = 4,5 to 18 V; V_{EE} = 0 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7)					
Supply current					
during normal operation, unloaded					
at V_{CC} = 4,5 V	I_{CC}	–	45	60	mA
at V_{CC} = 18 V	I_{CC}	–	50	70	mA
during power-on blanking, unloaded					
at V_{CC} = 4,5 V	I_{CC}	–	1,5	2	mA
at V_{CC} = 18 V	I_{CC}	–	5	7	mA
Supply voltage rise time to ensure power on reset		3	–	–	μs/V
Clock input CLK (pin 6)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,8	V
Input current					
HIGH at V_{CLKH} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{CLKL} = 0,4 V	$-I_{IL}$	–	–	10	μA
Clock pulse duration					
HIGH	t_{WH}	8	–	–	μs
LOW	t_{WL}	10	–	–	μs
DATA input (pin 4)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,8	V
Input current					
HIGH at V_{IH} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{IL} = 0,4 V	$-I_{IL}$	–	–	10	μA
DATA input in sink current					
ACK = TRUE	I_{DACK}	1	–	–	mA
Data line enable input DLEN (pin 5)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,8	V
Input current					
HIGH at $V_{5\text{-}3}$ = 2 V	I_{IH}	–	–	10	μA
LOW at $V_{5\text{-}3}$ = 0,4 V	$-I_{IL}$	–	–	10	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Outputs Q1 to Q13					
Output voltage during normal operation					
HIGH at $-I_{OH}$ = 80 mA	V_{OH}	V_{CC}−1,5	–	–	V
LOW at I_{OL} = 80 mA	V_{OL}	–	–	1	V
Output current during power-on reset					
HIGH	$-I_{OH}$	–	–	10	μA
LOW	I_{OL}	–	–	10	μA
Rise and fall times: no maximum					
Minimum times as V_{CC} = 4,5 volts (see Fig. 3)					
Set-up time ENABLE	t_{SUDL}	2,8	–	–	μs
Hold time ENABLE	t_{HDL}	5,0	–	–	μs
Set-up time DATA	t_{SDA}	0	–	–	μs
Hold time DATA	t_{HDA}	2,8	–	–	μs
Set-up time LOAD	t_{SLO}	1,4	–	–	μs
Pulse width LOW	t_{WL}	10	–	–	μs
Pulse width HIGH	t_{WH}	8	–	–	μs
Max. clock input frequency = $1/(t_{WH} + t_{WL})$	f_{max}	–	–	50	kHz
Propagation delay					
clock to outputs	t_{PCQ}	–	–	8,5	μs
acknowledge	t_{PCA}	–	–	6	μs
acknowledge release	t_{PCAR}	–	–	6	μs

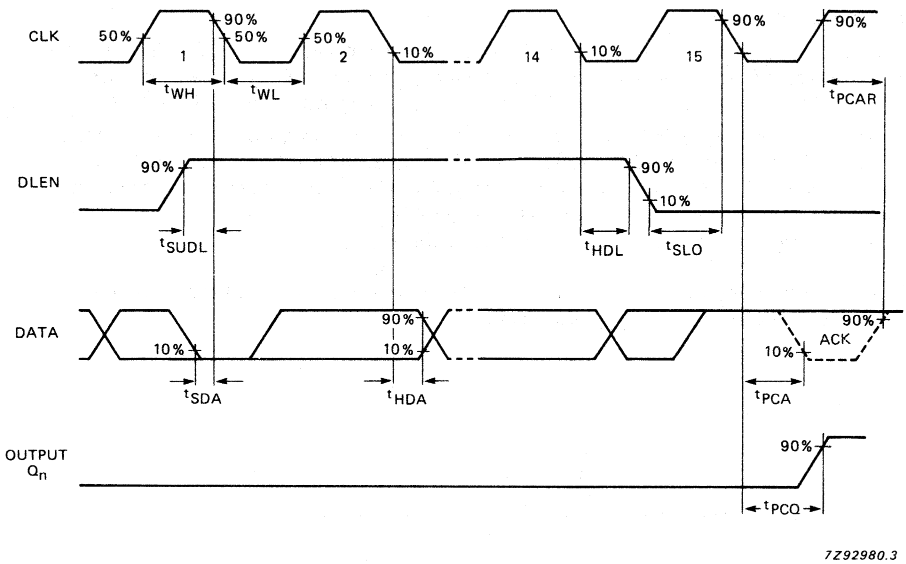


Fig. 3 Bus timing characteristics.

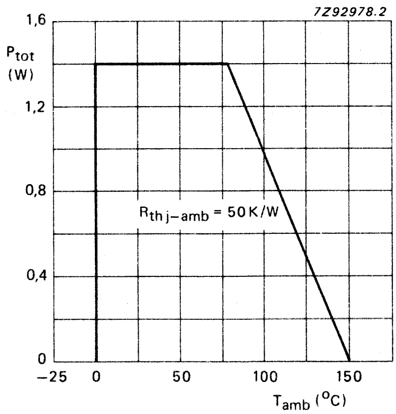


Fig. 4 Derating curve.

APPLICATION INFORMATION

1. From the buffer-capacitors C1 of the power supply the supply connections to the TEA1017 and the loads should be separated. An extra capacitor of 10 μF with good high-frequency characteristics should be mounted across the V_{CC} and V_{EE} connections as close as possible to the TEA1017.
2. If no use is made of the acknowledge information it is advised to program the data-output from the controller to LOW during the time ACK is valid. To use the acknowledge information the data-output has to be programmed HIGH. When a push-pull controller device is used a series resistor has to be connected in the data-line between the controller and TEA1017.
   The ACK may be sensed on the TEA1017-side of this resistor. See Fig. 5.

Note. ACK is removed from the data-line after the next LOW-to-HIGH transition of the clock-line with a maximum delay of 6 μs. (t_{PCA} maximum).

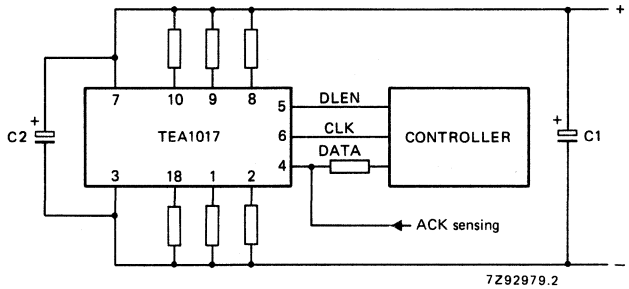


Fig. 5 TEA1017 with 3 loads to V_{CC} Q = 0 and 3 loads to V_{EE} Q = 1.

CONTROL CIRCUIT FOR SWITCHED-MODE POWER SUPPLY

GENERAL DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g. a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

It has the following features:

- Suited for frequency and duty factor regulation.
- Suited for flyback converters and forward converters.
- Wide frequency range.
- Adjustable input sensitivity.
- Adjustable minimum frequency or maximum duty factor limit.
- Adjustable overcurrent protection limit.
- Supply voltage out-of-range protection.
- Slow-start facility.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom.	14	V
Supply current	I_{CC}	max.	13	mA
Output pulse repetition frequency range	f_o		1 Hz to 100	kHz
Output current LOW	I_{OL}	max.	1	A
Operating ambient temperature range	T_{amb}		−25 to +125	^oC

7

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

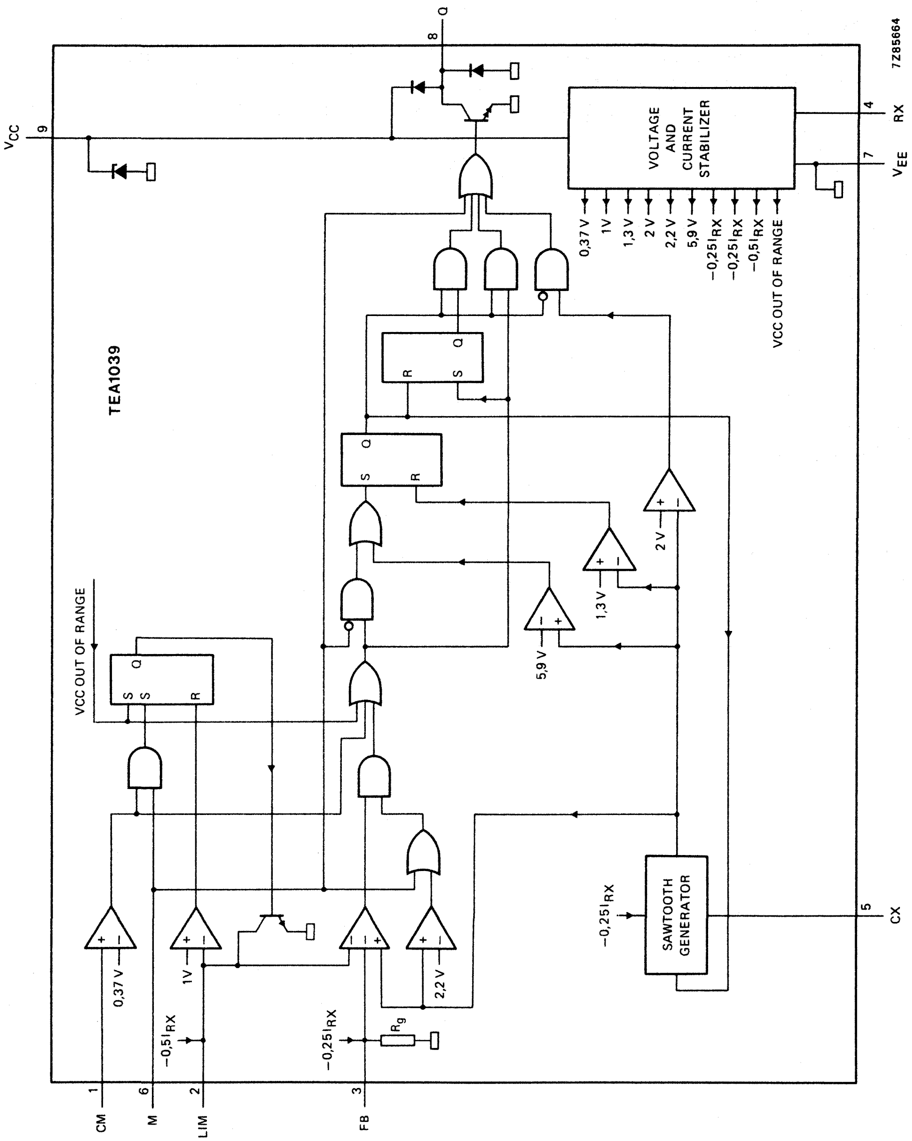


Fig. 1 Block diagram.

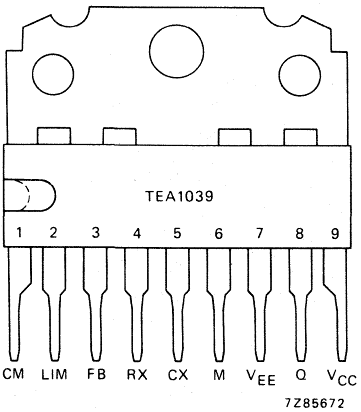


Fig. 2 Pinning diagram.

PINNING

1	CM	overcurrent protection input
2	LIM	limit setting input
3	FB	feedback input
4	RX	external resistor connection
5	CX	external capacitor connection
6	M	mode input
7	V_{EE}	common
8	Q	output
9	V_{CC}	positive supply connection

FUNCTIONAL DESCRIPTION

The TEA1039 produces pulses to drive the transistor in a switched-mode power supply. These pulses may be varied either in frequency (frequency regulation mode) or in width (duty factor regulation mode).

The usual arrangement is such that the transistor in the SMPS is ON when the output of the TEA1039 is HIGH, i.e. when the open-collector output transistor is OFF. The duty factor of the SMPS is the time that the output of the TEA1039 is HIGH divided by the pulse repetition time.

Supply V_{CC} (pin 9)

The circuit is usually supplied from the SMPS that it regulates. It may be supplied either from its primary d.c. voltage or from its output voltage. In the latter case an auxiliary starting supply is necessary.

The circuit has an internal V_{CC} out-of-range protection. In the frequency regulation mode the oscillator is stopped; in the duty factor regulation mode the duty factor is made zero. When the supply voltage returns within its range, the circuit is started with the slow-start procedure.

When the circuit is supplied from the SMPS itself, the out-of-range protection also provides an effective protection against any interruption in the feedback loop.

Mode input M (pin 6)

The circuit works in the frequency regulation mode when the mode input M is connected to ground (V_{EE}, pin 7). In this mode the circuit produces output pulses of a constant width but with a variable pulse repetition time.

The circuit works in the duty factor regulation mode when the mode input M is left open. In this mode the circuit produces output pulses with a variable width but with a constant pulse repetition time.

FUNCTIONAL DESCRIPTION (continued)

Oscillator resistor and capacitor connections RX and CX (pins 4 and 5)

The output pulse repetition frequency is set by an oscillator whose frequency is determined by an external capacitor C5 connected between the CX connection (pin 5) and ground (V_{EE}, pin 7), and an external resistor R_4 connected between the RX connection (pin 4) and ground. The capacitor C5 is charged by an internal current source, whose current level is determined by the resistor R4. In the frequency regulation mode these two external components determine the minimum frequency; in the duty factor regulation mode they determine the working frequency (see Fig. 4). The output pulse repetition frequency varies less than 1% with the supply voltage over the supply voltage range.

In the frequency regulation mode the output is LOW from the start of the cycle until the voltage on the capacitor reaches 2 V. The capacitor is further charged until its voltage reaches the voltage on either the feedback input FB or the limit setting input LIM, provided it has exceeded 2,2 V. As soon as the capacitor voltage reaches 5,9 V the capacitor is discharged rapidly to 1,3 V and a new cycle is initiated (see Figs 5 and 6).

For voltages on the FB and LIM inputs lower than 2,2 V, the capacitor is charged until this voltage is reached; this sets an internal maximum frequency limit.

In the duty factor regulation mode the capacitor is charged from 1,3 V to 5,9 V and discharged again at a constant rate. The output is HIGH until the voltage on the capacitor exceeds the voltage on the feedback input FB; it becomes HIGH again after discharge of the capacitor (see Figs 7 and 8). An internal maximum limit is set to the duty factor of the SMPS by the discharging time of the capacitor.

Feedback input FB (pin 3)

The feedback input compares the input current with an internal current source whose current level is set by the external resistor R4. In the frequency regulation mode, the higher the voltage on the FB input, the longer the external capacitor C5 is charged, and the lower the frequency will be. In the duty factor regulation mode external capacitor C5 is charged and discharged at a constant rate, the voltage on the FB input now determines the moment that the output will become LOW. The higher the voltage on the FB input, the longer the output remains HIGH, and the higher the duty factor of the SMPS.

Limit setting input LIM (pin 2)

In the frequency regulation mode this input sets the minimum frequency, in the duty factor regulation mode it sets the maximum duty factor of the SMPS. The limit is set by an external resistor R2 connected from the LIM input to ground (pin 7) and by an internal current source, whose current level is determined by external resistor R4.

A slow-start procedure is obtained by connecting a capacitor between the LIM input and ground. In the frequency regulation mode the frequency slowly decreases from f_{max} to the working frequency. In the duty factor regulation mode the duty factor slowly increases from zero to the working duty factor.

Overcurrent protection input CM (pin 1)

A voltage on the CM input exceeding 0,37 V causes an immediate termination of the output pulse. In the duty factor regulation mode the circuit starts again with the slow-start procedure.

Output Q (pin 8)

The output is an open-collector n-p-n transistor, only capable of sinking current. It requires an external resistor to drive an n-p-n transistor in the SMPS (see Figs 9 and 10).

The output is protected by two diodes, one to ground and one to the supply.

At high output currents the dissipation in the output transistor may necessitate a heatsink. See the power derating curve (Fig. 3).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, voltage source	V_{CC}	−0,3 to +20	V
Supply current range, current source	I_{CC}	−30 to +30	mA
Input voltage range, all inputs	V_I	−0,3 to +6	V
Input current range, all inputs	I_I	−5 to +5	mA
Output voltage range	$V_{8\text{-}7}$	−0,3 to +20	V
Output current range			
output transistor ON	I_8	0 to 1	A
output transistor OFF	I_8	−100 to + 50	mA
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range (see Fig. 3)	T_{amb}	−25 to +125	°C
Power dissipation (see Fig. 3)	P_{tot}	max. 2	W

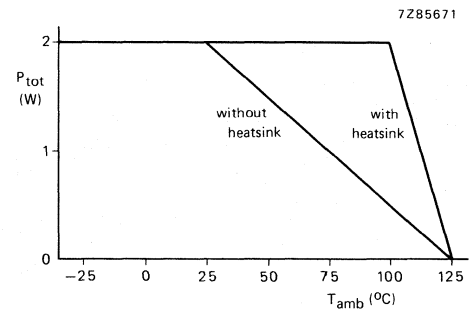


Fig. 3 Power derating curve.

7

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 9)					
Supply voltage, operating	V_{CC}	11	14	20	V
Supply current					
at V_{CC} = 11 V	I_{CC}	–	7,5	11	mA
at V_{CC} = 20 V	I_{CC}	–	9	12	mA
variation with temperature	$\frac{\Delta I_{CC}/I_{CC}}{\Delta T}$	–	–0,3	–	%/K
Supply voltage, internally limited					
at I_{CC} = 30 mA	V_{CC}	23,5	–	28,5	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	18	–	mV/K
Low supply threshold voltage	V_{CCmin}	9	10	11	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	–5	–	mV/K
High supply threshold voltage	V_{CCmax}	21	23	24,6	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	10	–	mV/K
Feedback input FB (pin 3)					
Input voltage for duty factor = 0; M input open	V_{3-7}	0	–	0,3	V
Internal reference current	$-I_{FB}$	–	0,5 I_{RX}	–	mA
Internal resistor R_g	R_g	–	130	–	kΩ
Limit setting input LIM (pin 2)					
Threshold voltage	V_{2-7}	–	1	–	V
Internal reference current	$-I_{LIM}$	–	0,25 I_{RX}	–	mA
Overcurrent protection input CM (pin 1)					
Threshold voltage	V_{1-7}	300	370	420	mV
variation with temperature	$\Delta V_{1-7}/\Delta T$	–	0,2	–	mV/K
Propagation delay, CM input to output	t_{PHL}	–	500	–	ns

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.	unit
Oscillator connections RX and CX (pins 4 and 5)					
Voltage at RX connection at $-I_4$ = 0,15 to 1 mA	$V_{4\text{-}7}$	6,2	7,2	8,1	V
variation with temperature	$\Delta V_{4\text{-}7}/\Delta T$	–	2,1	–	mV/K
Lower sawtooth level	V_{LS}	–	1,3	–	V
Threshold voltage for output H to L transition in F mode	V_{FT}	–	2	–	V
Threshold voltage for maximum frequency in F mode	V_{FM}	–	2,2	–	V
Higher sawtooth level	V_{HS}	–	5,9	–	V
Internal capacitor charging current, CX connection	$-I_{CX}$	–	$0{,}25\, I_{RX}$	–	mA
Oscillator frequency (output pulse repetition frequency)	f_o	1	–	10^5	Hz
Minimum frequency in F mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Maximum frequency in F mode, initial deviation	$\Delta f/f$	−20	–	+20	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	−0,16	–	%/K
Output LOW time in F mode, initial deviation	$\Delta t/t$	−25	–	+25	%
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Pulse repetition frequency in D mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Minimum output LOW time in D mode at C_5 = 3,6 nF	t_{OLmin}	–	1	–	μs
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Output Q (pin 8)					
Output voltage LOW at I_8 = 100 mA	$V_{8\text{-}7}$	–	0,8	1,2	V
variation with temperature	$\Delta V_{8\text{-}7}/\Delta T$	–	1,5	–	mV/K
Output voltage LOW at I_8 = 1 A	$V_{8\text{-}7}$	–	1,7	2,1	V
variation with temperature	$\Delta V_{8\text{-}7}/\Delta T$	–	−1,4	–	mV/K

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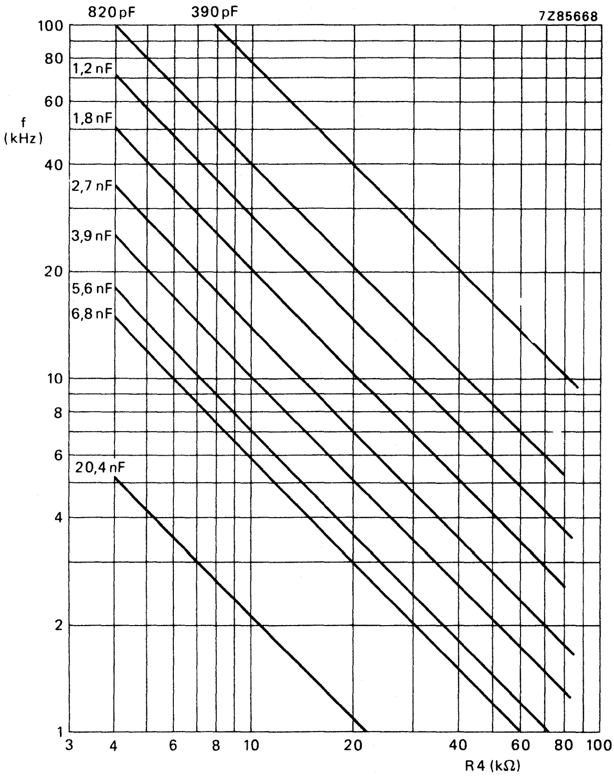

Fig. 4 Minimum pulse repetition frequency in the frequency regulation mode, and working pulse repetition frequency in the duty factor regulation mode, as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

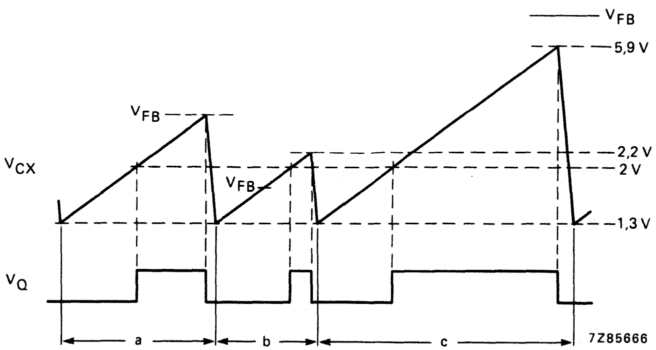

Fig. 5 Timing diagram for the frequency regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for three combinations of input signals. *a:* The voltages on inputs FB or LIM are between 2,2 V and 5,9 V. The circuit is in its normal regulation mode. *b:* The voltage on input FB or input LIM is lower than 2,2 V. The circuit works at its maximum frequency. *c:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit works at its minimum frequency.

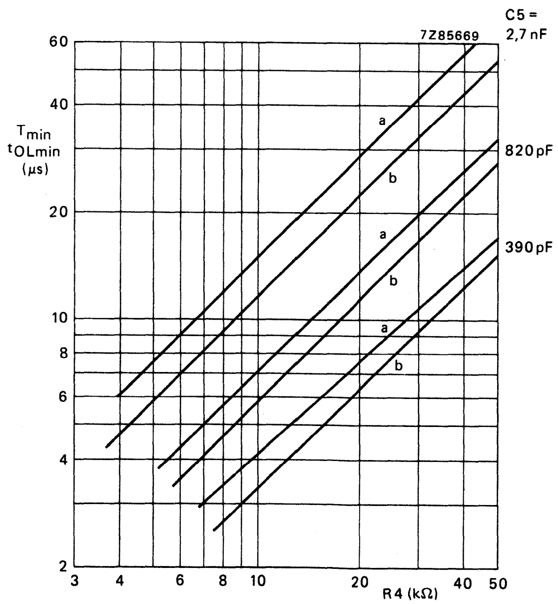

Fig. 6 Minimum output pulse repetition time T_{min} (curves a) and minimum output LOW time t_{OLmin} (curves b) in the frequency regulation mode as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

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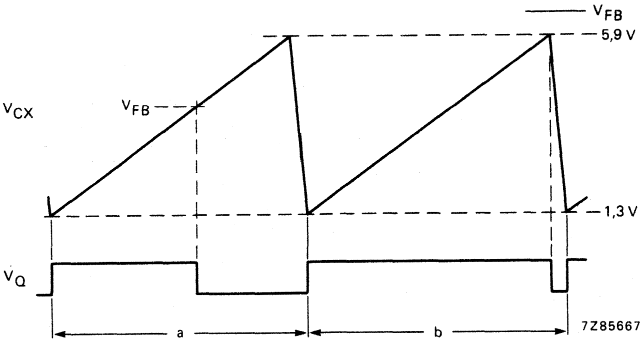

Fig. 7 Timing diagram for the duty factor regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for two combinations of input signals. *a:* The voltages on inputs FB or LIM are below 5,9 V. The circuit is in its normal regulation range. *b:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit produces its minimum output LOW time, giving the maximum duty factor of the SMPS.

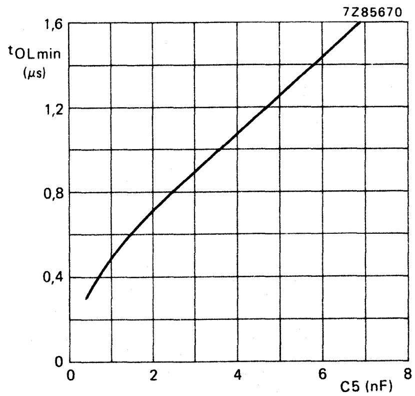

Fig. 8 Minimum output LOW time t_{OLmin} in the duty factor regulation mode as a function of external capacitor C5 connected between CX and ground. In this mode the minimum output LOW time is independent of R4 for values of R4 between 4 kΩ and 80 kΩ.

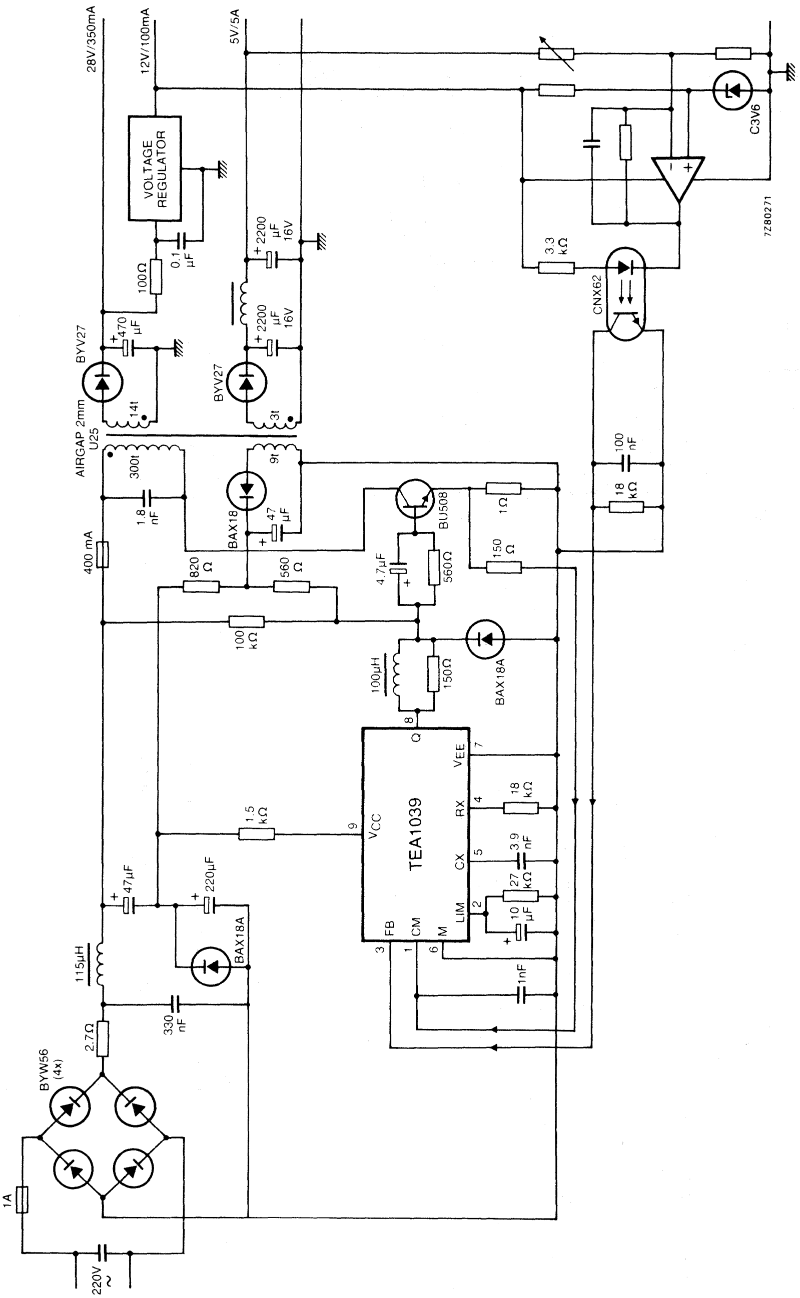

Fig. 9 Typical application of the TEA1039 in a variable-frequency flyback converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

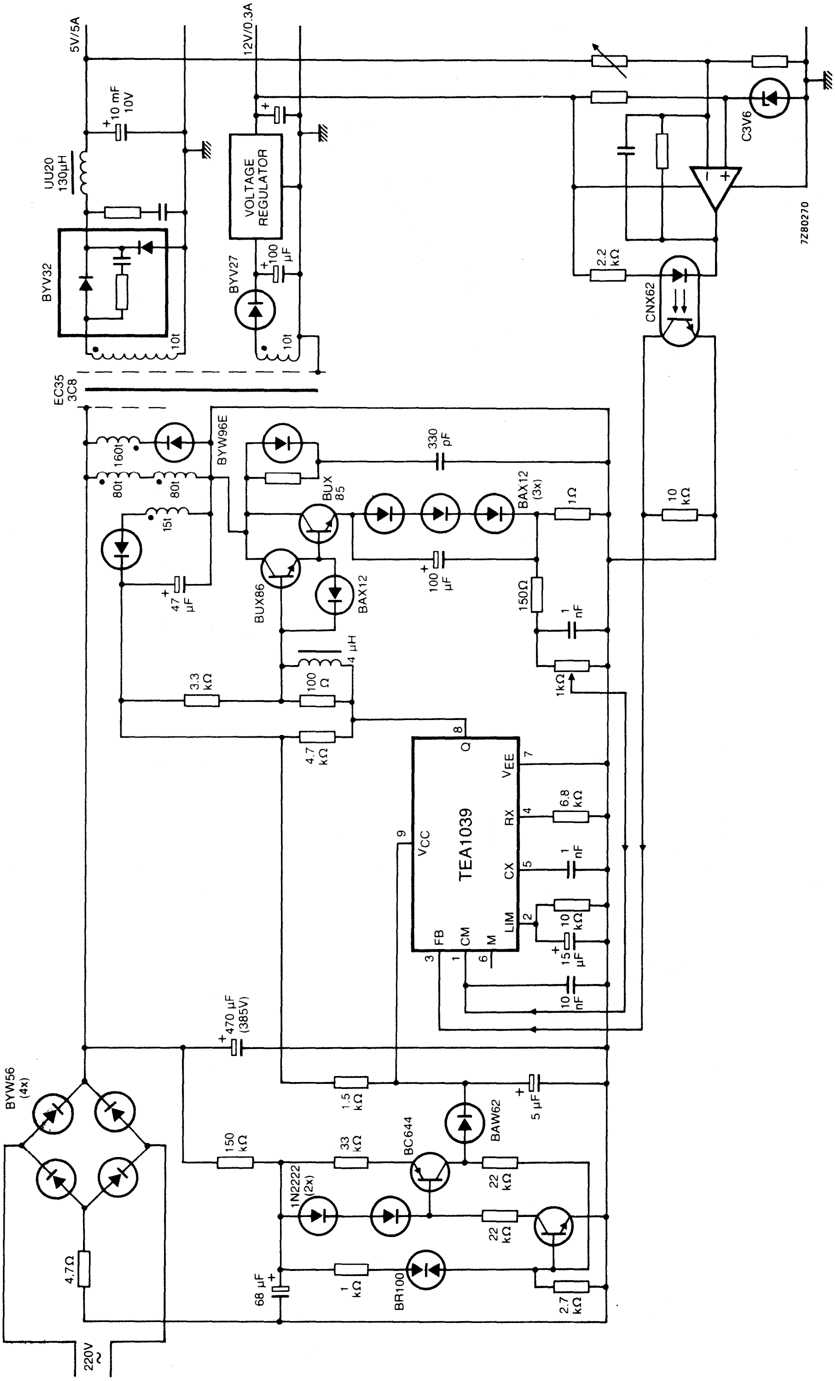

Fig. 10 Typical application of the TEA1039 in a fixed-frequency, variable duty factor forward converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

Section 8
Applications

INDEX

SECTION 8 – APPLICATIONS

Designing With The SA/NE602

INTRODUCTION

The SA/NE602 represents a new industry standard for low power, double-balanced mixers. This device also includes an on-board local oscillator and voltage regulator. Typical power supply requirements are 2.5mA at 6 volts for a conversion gain of 20dB and a noise figure of 5dB with operation up to 200MHz. The SA/NE602 is available in either an eight pin DIP or a surface mount package. These specifications render this device an ideal choice for portable battery-operated applications.

CIRCUIT CONFIGURATIONS

Figure 1 shows a simplified block diagram of the SA/NE602. A multiplier "Gilbert Cell" is used as the mixer portion of the device with the input differential amplifier providing most of the conversion gain. This differential amplifier also serves as an input balun which helps reduce the second-order distortion products.

Figure 2 shows some possible balanced and unbalanced input and output circuits while Table 1 summarizes these configurations' relative advantages and disadvantages.

Figure 3 shows the internal circuitry adjacent to the device pins. The oscillator can be configured with a crystal, a tank, or as a buffer/driver for an external oscillator. When used as a buffer amplifier, optimum performance will be achieved when pin 6 is driven with a 200 to 300mV RMS signal. This LO amplitude tolerance becomes more critical as the LO frequency approaches the 200MHz maximum. Figure 4 shows a typical test circuit for the SA/NE602. For this circuit it is important to specify the *parallel mode* crystal frequency and use a crystal with a loading capacitance of 5pF.

DESIGN DATA

Figure 6 shows typical intermodulation and compression point performance of the SA/NE602. The compression point defines the upper limit of the effective mixer dynamic range at about −25dBm. This level is mainly a function of the circuit insertion loss prior to the 602 input. The input third order intercept point is shown here at the minimum value of −15dBm, and, as such, can be considered a worst case condition.

The remaining charts show various mixer parameters over temperature and supply voltage variation. The overall optimum supply voltage is 6 volts, and this value is thus recommended. Unless specifically indicated, Figure 4 was the test circuit used to produce the data. The frequency schemes used here are typical of those found in cellular radio applications employing a 455kHz 2nd IF. All of the major specifications are nearly constant over the 200MHz frequency range with the exception of the LO drive level tolerance and device impedances.

OSCILLATOR ALIGNMENT

The objective in measuring the crystal oscillator frequency in a production environment is to read the data without loading the circuit. This can be accomplished by using one of two methods. The first uses a small inductive loop placed near the oscillator circuit. The loop feeds a suitable amplifier which drives a counter. The second method takes advantage of LO leakage into the output. Again, with the oscillator running and no RF input signal present, the 602 output is connected to an amplifier and counter. The single-ended output configuration will provide more LO leakage and the mixer itself will act as a buffer.

Written by: Bob Zavrel

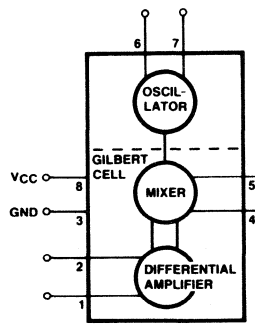

Figure 1. SA/NE602 Functional Diagram

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Designing With The SA/NE602

AN198

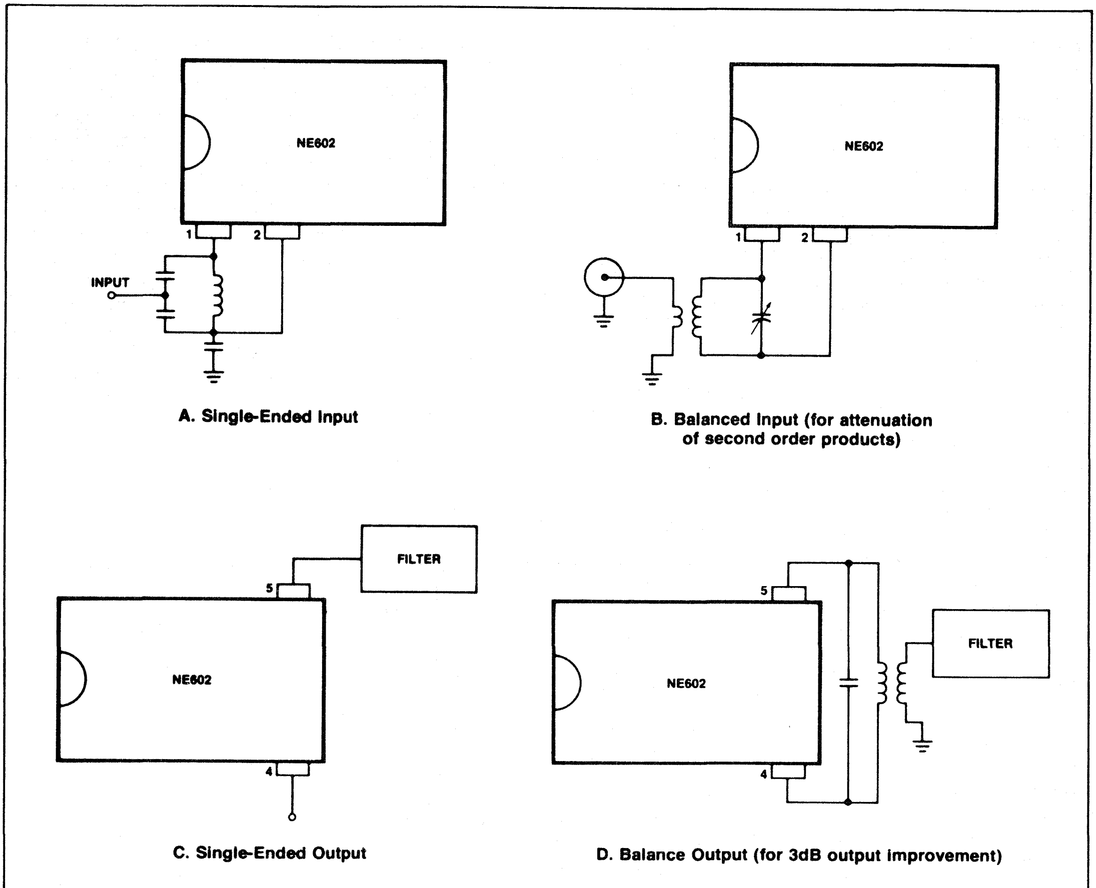

Figure 2. Circuit Configurations

TABLE 1

		ADVANTAGES	DISADVANTAGES
Input Pins 1 & 2	Single-ended	No sacrifice in 3rd order performance, simplified circuit	Increase in 2nd order products
	Balanced	Reduce 2nd order products	Impedance match more difficult to achieve
Output Pins 4 & 5	Single-ended	Simple interface to filters	3dB reduction in output, less RF and LO isolation
	Balanced	3dB improvement in output, better LO and RF isolation at the output	more complex circuitry required

Designing With The SA/NE602

AN198

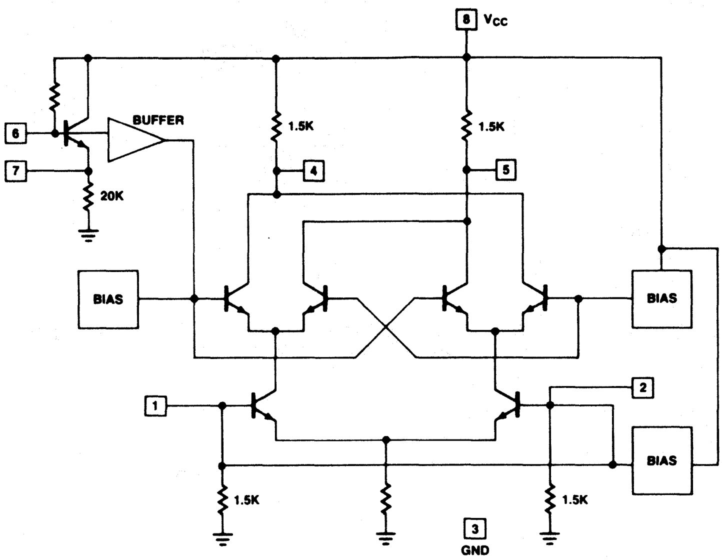

Figure 3. SA/NE602 Equiv Circuit

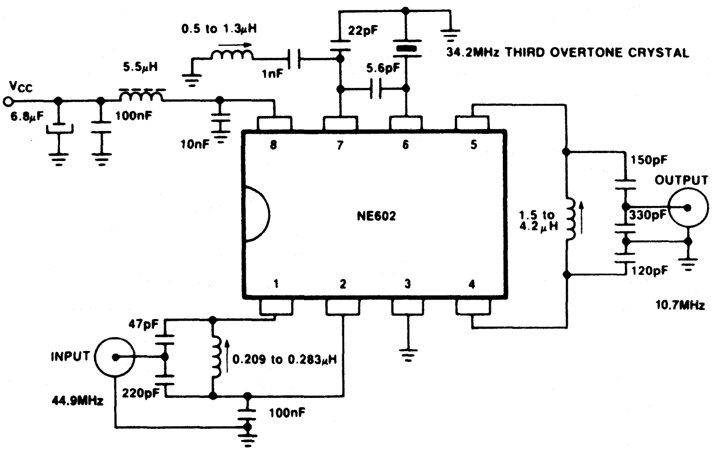

Figure 4. Typical Application

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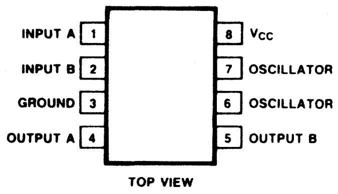
D, N PACKAGES



ORDER PART NUMBERS

NE602N SA602N
NE602D SA602D

Figure 5. Pin Configuration

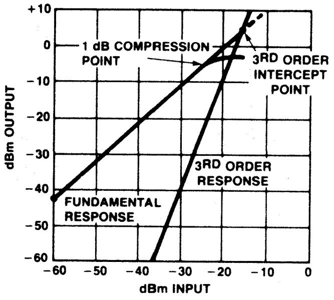


Figure 6. SA/NE602 3RD Order Intermod and 1dB Compression Point Performance

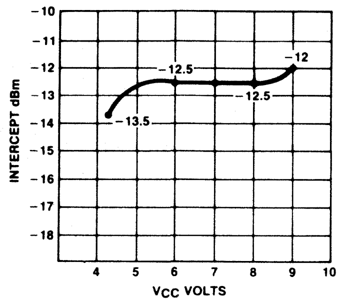


Figure 7. Input Third Order Intercept Point Vs V_{CC}

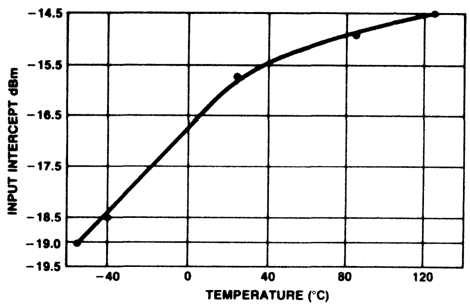


Figure 8. Third Order Intercept Point Vs Temperature

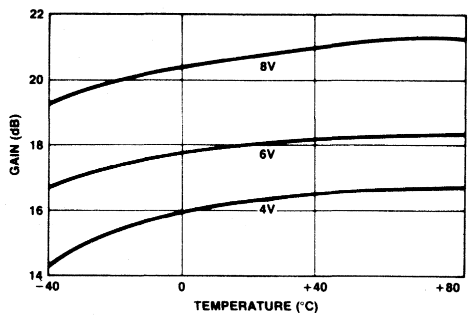


Figure 9.

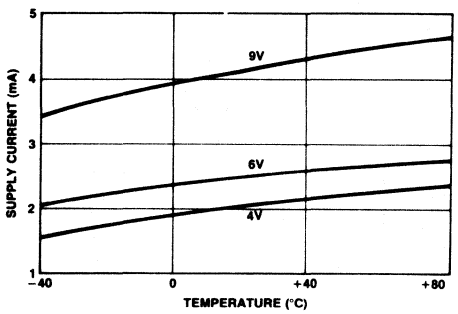


Figure 10.

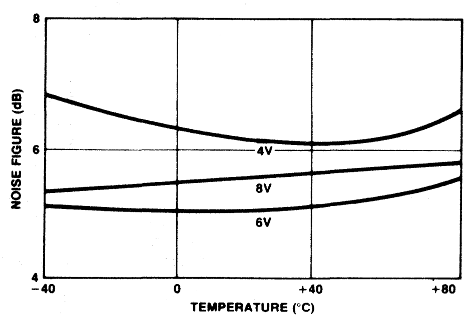


Figure 11.

Designing with the SA/NE604

AN199

INTRODUCTION

The SA/NE604 represents a new standard of performance in low power FM IF integrated circuits. Originally designed for cellular radio applications, the 604 is also well suited to other radio frequency circuits where good performance and low power consumption are the important design considerations. When used with its companion double-balanced mixer, the SA/NE602, a low power system solution for the cellular radio and other RF applications is realized. (Reference 1).

Figures 1 and 2 show the device pin-out and a functional diagram of the 604. The device provides an IF amplifier, quadrature detector, received signal strength indicator (RSSI), and mute circuit. Two detector outputs are provided for audio and data information with the audio output being controlled by the mute circuit.

CIRCUIT OVERVIEW

The IF amplifier consists of five differential stages with a total gain of about 90dB. Provision is made for an external inter-stage filter to reduce broadband noise and increase receiver selectivity. The differential input to the first IF section appears at pins 15 and 16. One pin is usually AC-coupled to ground (pin 15) with pin 16 used as the "high" input. The first IF section has a typical gain of 40dB with its output appearing on pin 14. Similar to the first IF section, the second section uses a differential input appearing at pins 12 and 11, with pin 11 usually AC-coupled to ground. The five stages are identical and any one may go into limiting, depending on the RF input level.

The interstage filter can be ceramic, crystal, or an LC circuit. RSSI tracking is optimized when the filter circuit loss is 6dB. The output impedance of both amplifier sections (pins 14 and 9) is about 1K ohms. For convenience, an "L" pad circuit showing 6dB loss is shown in Figure 3. This circuit allows observation of the RSSI response without using a filter.

The quadrature detector multiplies two IF signals to produce the audio output. One of the IF signals is differentially phase shifted by an external quadrature tank or discriminator circuit connected between pins 8 and 9 (Figure 4). The second IF signal is fed to the other detector input internally. Figure 5 shows the desired phase/frequency response of the quadrature-tuned circuit. A detailed mathematical explanation of detector operation can be found in Reference 2. The detected audio appears at the data terminal (pin 7) and, via the mute circuit, at the audio (pin 6) terminal.

The cellular radio specifications call for a logarithmic signal strength indicator accurate within 3dB over an 80dB dynamic range. The 604 meets this requirement with an effective technique. A sample current corresponding to the output of each IF stage is fed to a summing amplifier. The output of this amplifier provides a current source which is reflected by a current mirror. The current mirror output that appears on pin 5 provides the logarithmic RSSI information. It is usable over a 90dB dynamic range with 1.5dB accuracy. Typically, a 100K ohm resistor is used to convert the RSSI current to a voltage which is logarithmically proportional to the received signal strength.

PACKAGING

Both the SA/NE604 and its companion double balanced mixer, the SA/NE602, are available in either the plastic dual-in-line "DIP" or surface mounted "SO" packages. The NE prefix specifies a 0 to+70°C operating temperature range while SA specifies−40 to+85°C operation. The extensive temperature data presented in this application note pertain to both the SA and NE devices.

TYPICAL APPLICATIONS

Figure 6 is a simplified schematic diagram of the 604 which details the internal circuitry adjacent to the device's pins. This should help the designer match impedances to external circuitry. Figure 7 shows the schematic diagram of a typical test circuit using the 604 and 602.

The quadrature tuned circuit (F3) shifts the phase of the IF signal as shown in Figure 5. Low distortion demodulation is obtained if the IF signal deviation is restricted to the linear portion of the S-curve. There are three variables affecting quadrature linearity: circuit Q, deviation, and IF frequency. If the deviation is increased, the Q must be decreased for a given degree of linearity. The circuit Q will also affect the demodulated signal level. A higher Q will yield a higher audio output from the quadrature detector since the phase shift will be greater for a given deviation. The quadrature Q must be optimized for a given frequency deviation, IF frequency, and desired linearity. A loaded Q of about 20 is typical for narrow band FM applications using a 455kHz IF.

The supply voltage for the 602/604 pair can range from 4.5 to 8 volts. Optimum overall performance is realized at 6.0 volts for the device pair. Several operation parameters are plotted for supply voltage as well as temperature.

Quadrature detector linearity can be affected by temperature variations. LC circuit resonances will drift as the coil and capacitor values change with temperature. This effect becomes more critical with increased circuit Q. If wide temperature variations are expected, careful choice of circuit components can minimize this effect. Most inductors have positive temperature coefficients (increase of inductance with increase of temperature). If a negative coefficient capacitor is chosen to compensate the inductor, the resonant frequency will track over temperature.

Since a bipolar current source is used to provide the RSSI function, the current will change with temperature. An increase in temperature will result in an increase in RSSI indication (Figure 8, uncorrected response). The circuit shown in Figure 9 will "smooth" the response over temperature by dropping the load impedance presented to pin 5 as temperature increases (Figure 8, corrected response).

All the major performance parameters of the 604 are shown in Figure 10. Figure 11 illustrates a typical test set-up for measuring many of the discussed parameters. Figures 12 to 25 provide a comprehensive guide to 604 performance over temperature and other variables.

USE AS A FIELD STRENGTH/ RF VOLTMETER

As stated earlier the RSSI function is usable over a 90dB dynamic range. This function taken alone can provide a useful RF voltmeter function. The circuit in Figure 26 can be used as a field strength or RF voltmeter application. A linear readout device can be calibrated directly in decibels or logarithmically for power, current, or volts.

USE AS AN AM SYNCHRONOUS DETECTOR

The 604 can also be used as an AM envelope detector. The IF signal is fed to both the 604,

Designing With The SA/NE604 AN199

as in the FM application, and to an additional linear IF amplifier (Figure 27). The linear amplifier then feeds the quadrature detector which mixes with the AM limited carrier and demodulates the envelope. 1% THD is obtainable with this technique with a 90% AM modulated signal.

USE AS A PRODUCT DETECTOR

Figure 28 shows how the 604 can be used as a product detector for SSB or DSB. In this case the LO is applied to the 604 IF amplifier and an external linear IF amplifier is used for the SSB or DSB signal. The 604 quadrature detector then acts as the product detector. With the addition of a simple switching array, a single 604 can be used for FM, AM, or SSB detection in a communications receiver!

REFERENCES

1. Zavrel, R.: Signetics AN198 *Designing With the SA/NE 602*, December, 1984.

2. Hayward, W.: *Introduction to Radio Frequency Design*, 1982, Prentice-Hall.

Written by Bob Zavrel

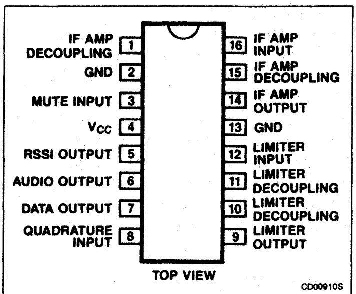


Figure 1. Pin Configuration

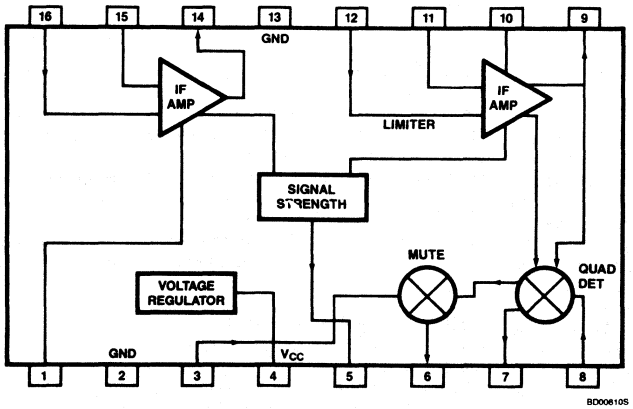


Figure 2. Block Diagram

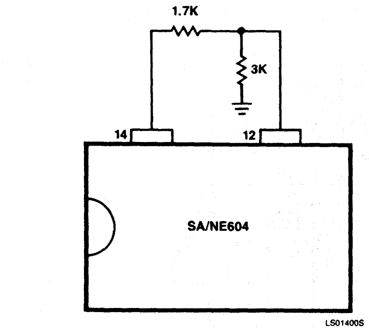


Figure 3. 6dB "L" Pad

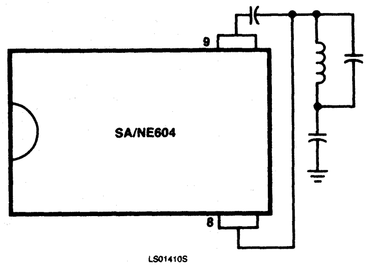


Figure 4. Quadrature Network

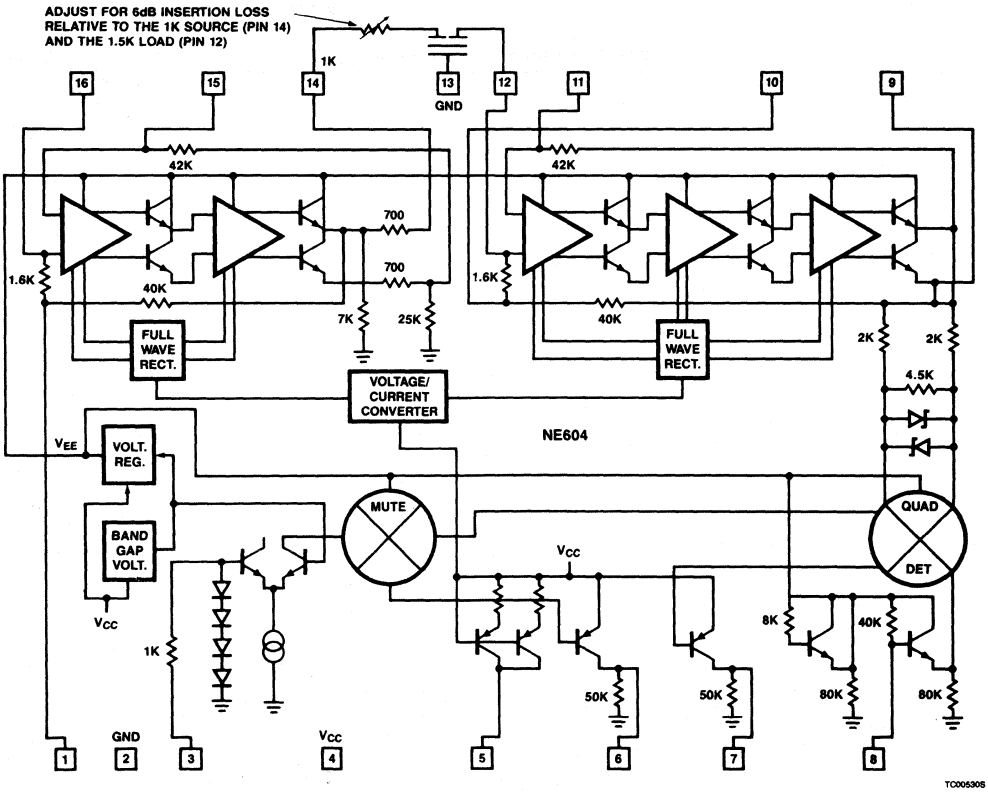


Figure 5.

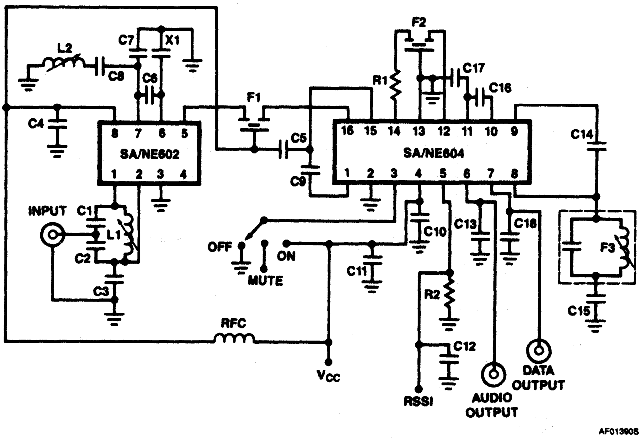


Figure 6. Application Demonstration Board

C1	47 pF ± 2%	100 V	N750 Ceramic
C2	220 pF ± 2%	100 V	N750 Ceramic
C3	0.1 μF ± 10%	50 V	Polyester
C4	10 nF ± 80% 20%	63 V	K10000 — 25X Ceramic
C5	0.1 μF ± 10%	50 V	Polyester
C6	5.6 pF ± 25%	100 V	NPO Ceramic
C7	22 pF ± 2%	100 V	N150 Ceramic
C8	1 nF ± 10%	100 V	K2000 — Y5P Ceramic
C9	0.1 μF ± 10%	50 V	Polyester
C10	0.1 μF ± 10%	50 V	Polyester
C11	6.8 μF ± 20%	25 V	Tantalum
C12	1 nF ± 10%	100 V	K2000 — Y5P Ceramic
C13	15 nF ± 10%	50 V	Polyester
C14	10 pF ± 2%	100 V	NPO Ceramic
C15	0.1 μF ± 10%	50 V	Polyester
C16	0.1 μF ± 10%	50 V	Polyester
C17	0.1 μF ± 10%	50 V	Polyester
C18	150 pF ± 2%	100 V	N1500 Ceramic
R1	1.5 K ± 5%	1/8 W	Carbon Composition
R2	100 K ± 1%	1/4 W	Metal Film
RFC	5.5 μH	RF Chocke J.W. Miller 542 — 4609	
L1	0.209 — 0.283 μH	Adjustable VHF Coil Miller 48A257MPC	
L2	0.5 — 1.3 μH	Adjustable Coil 1811 — 0036TW	
F1	455 kHz	Ceramic Filter Murata SFG 455A3	
F2			
F3	455 kHz	IF Filter Toko A2549	
X1	44.545 MHz	Third Overtone Crystal	

TB00440S

Figure 7. Application Test Board Parts

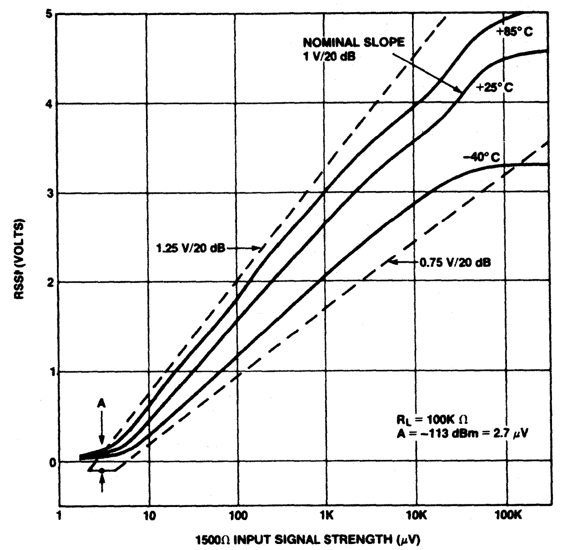


Figure 8. RSSI vs. Signal Strength

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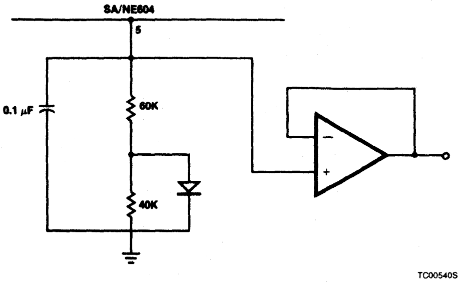


Figure 9. Temperature Compensated RSSI Circuit

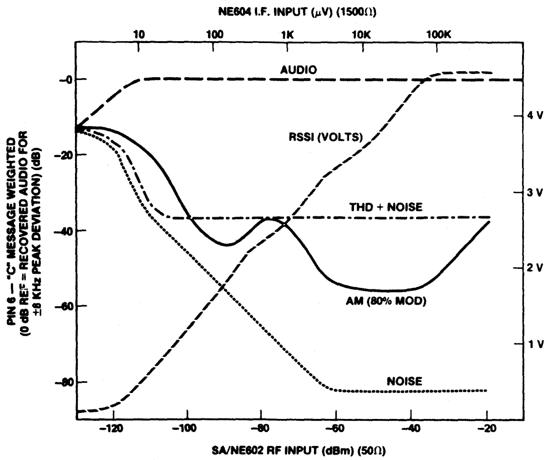


Figure 10. NE602/604 System Performance

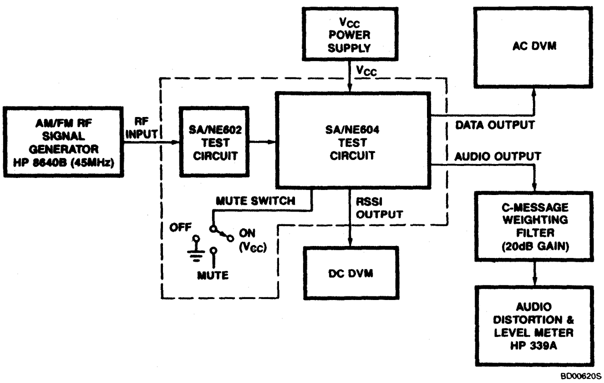


Figure 11. SA/NE602/SA/NE604 Applications Board

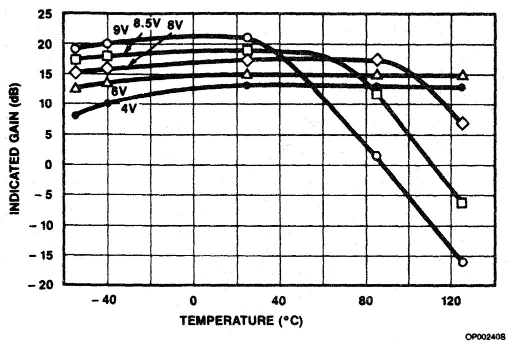


Figure 12. SA/NE604 Indicated Gain vs Temperature and Voltage

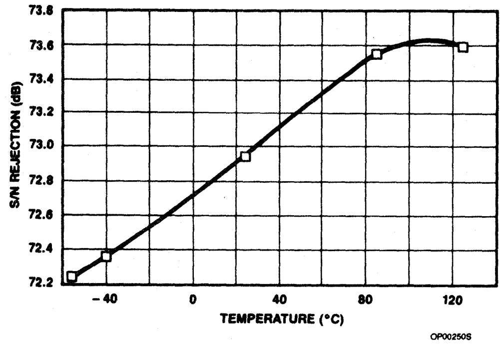


Figure 13. SA/NE604 Signal-To-Noise Ratio vs Temperature

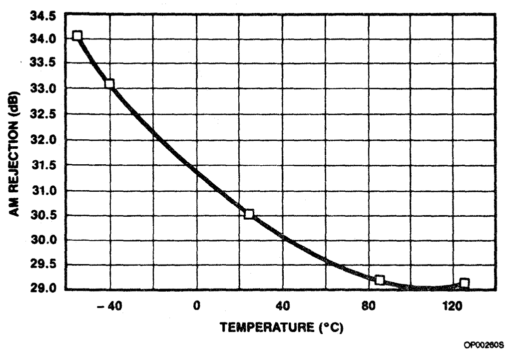


Figure 14. SA/NE604 AM Rejection vs Temperature

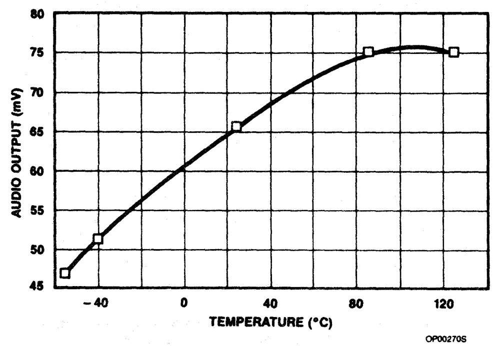


Figure 15. SA/NE604 Audio Output vs Temperature

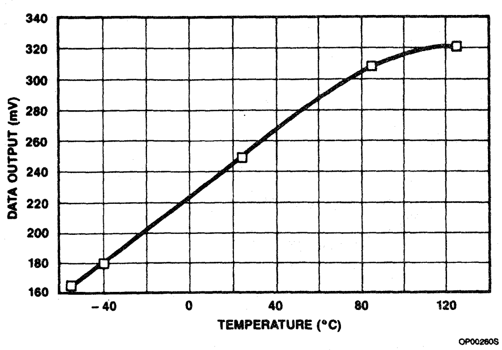


Figure 16. SA/NE604 Data Output vs Temperature

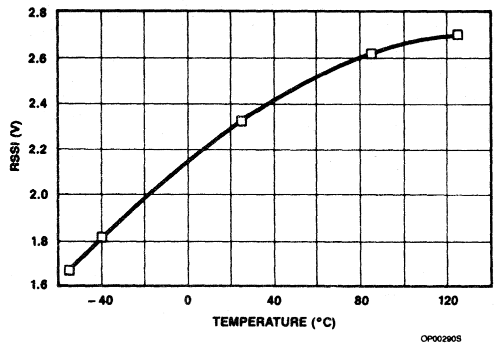


Figure 17. RSSI vs Temperature

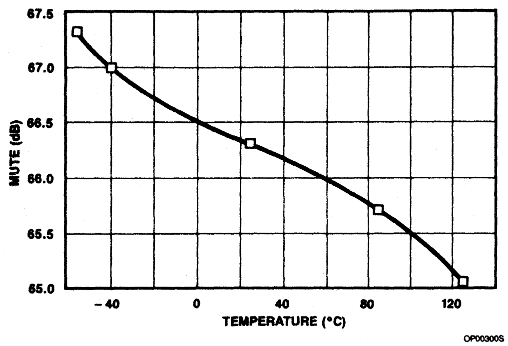


Figure 18. SA/NE604 Muting vs Temperature

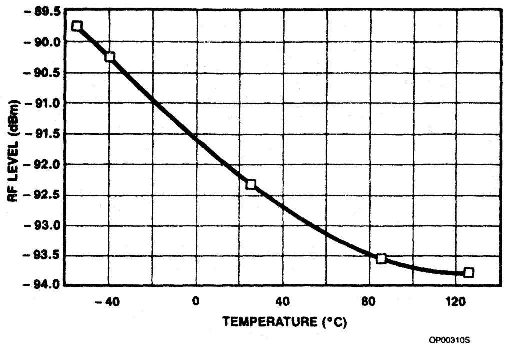


Figure 19. SA/NE604 Limiting RF Level vs Temperature

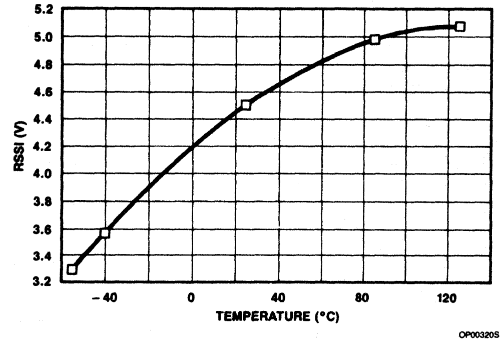


Figure 20. SA/NE604 Large Signal Uncompensated RSSI Voltage vs Temperature

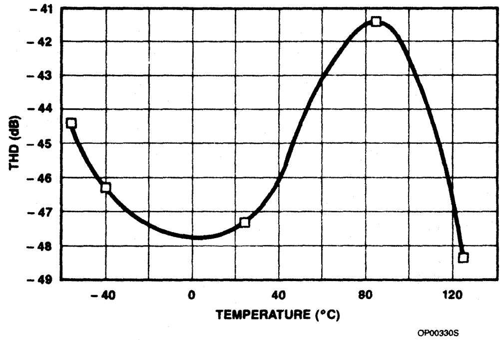


Figure 21. SA/NE604 Total Harmonic Distortion vs Temperature

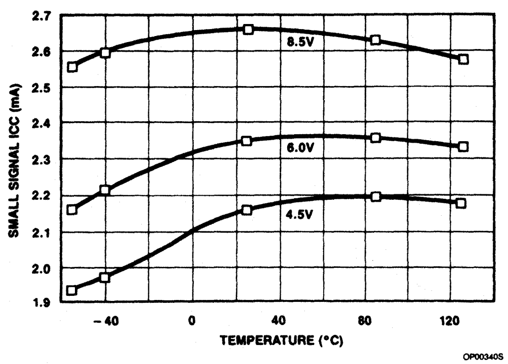


Figure 22. SA/NE604 Supply Current vs Temperature and Voltage

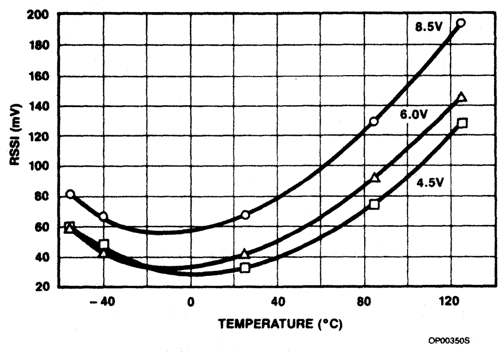


Figure 23. Small Signal RSSI vs Temperature and Voltage

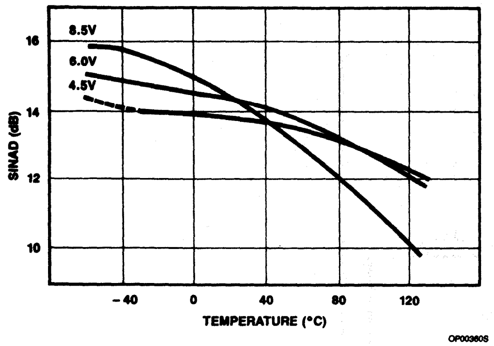


Figure 24. SA/NE604 SINAD vs Temperature and V_{CC}

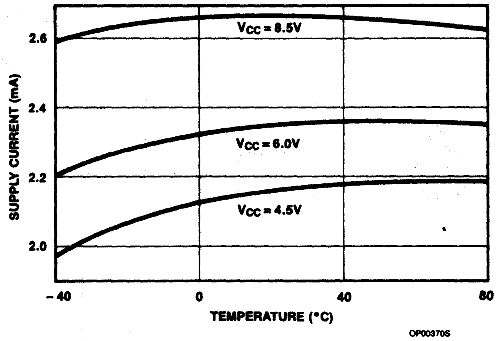


Figure 25. SA604 Supply Current vs Temperature

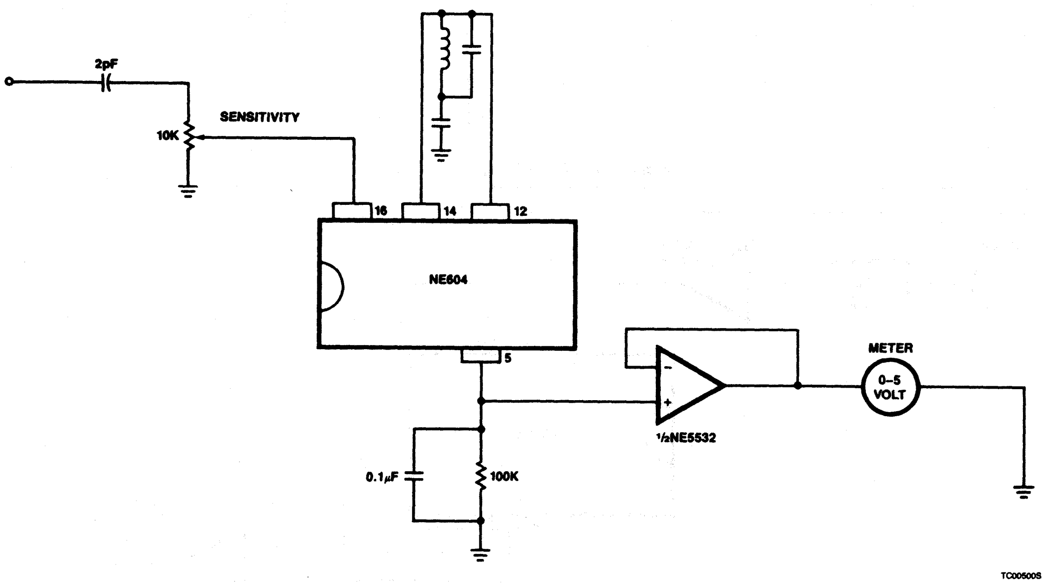


Figure 26. Field Strength Meter

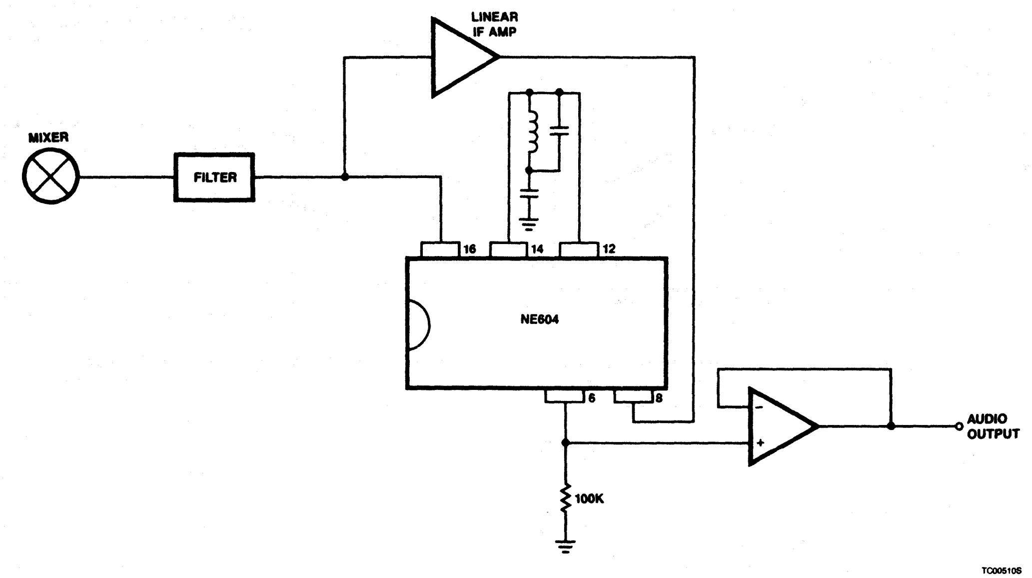


Figure 27. AM Synchronous Detector

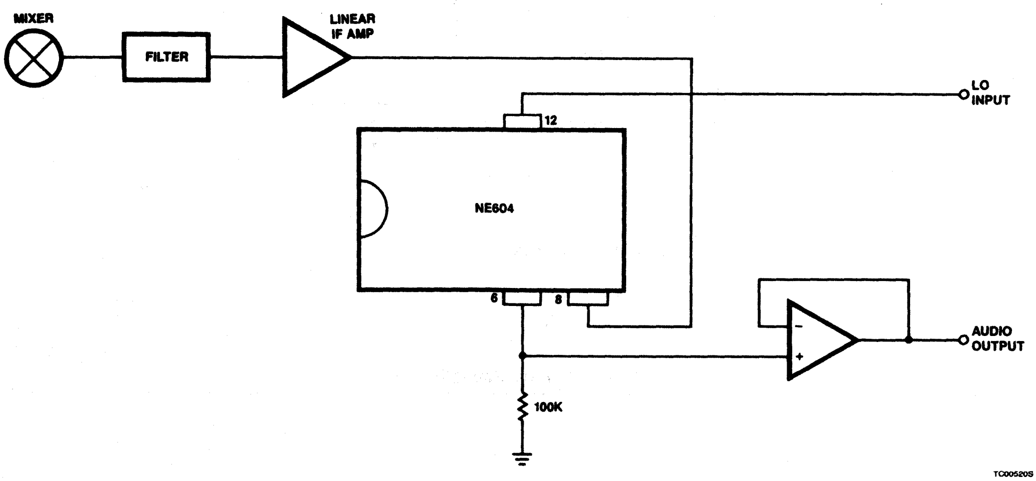


Figure 28. Product Detector

Wideband FM Composite Video Fiber Optic Link

AN146

INTRODUCTION

A low cost yet high performance, color, composite video fiber optic link for short-haul applications can easily be built using readily available off-the-shelf I.C.'s and optoelectronic devices. Also, all the necessary tools and hardware for interfacing the fiber to the electronics are available in kit form. This adds further simplicity and lower cost to the construction of the finished design and cancels the need to obtain factory installed terminations.

OPERATION

Starting at the transmitter end (Figure 1), the system begins with an NE592 differential video amplifier. The amplifier receives the composite video signal and then differentially drives the voltage controlled oscillator (VCO) of an NE564 phase locked loop (PLL). This is done through the output pins of the PLL phase comparator. The VCO is driven directly to avoid the input limiter and phase detector of the NE564. This method of operation opens up a number of applications for the NE564 that were previously impossible. The loop, in this case, is configured as a frequency modulator with a center of 30MHz and a deviation of ±10MHz. From here, the modulated signal is fed to an NE522 high speed comparator with an open collector output. The comparator boosts the signal in order to drive a high power aluminum gallium arsenide infrared (810μm) LED which has a typical rise time of 3ns.

The composite video is essentially sent at a 60 Mb/s data rate over the fiber and is received by an AlGaAs PIN photodiode. The light is converted to a current by the diode and is amplified and changed to a voltage by the NE5539 op amp in a transimpedance configuration. The very high speed response (600V/μs) and wide bandwidth (350MHz unity gain) makes this device ideally suited for high performance optical links. Compensation components and their values are also shown in Figure 1 to make the NE5539 unconditionally stable because it is not internally compensated. The second NE5539 is a voltage gain stage and is optional depending upon the attenuation in the fiber or its length. Immediately following is another NE564 PLL set up as an FM demodulator which is AC coupled to the last NE5539 op amp. This third NE5539 acts as an amplifier and buffer that drives 75 ohm cable to a video monitor.

TEST

Tests using 30 meters of 125μm glass fiber show the chrominance S/N ratio of an EIA color bar test signal to be approximately 40dB. This S/N ratio can be improved if an additional filter is added to the circuit. The primary noise source is the 30MHz modulation frequency. To attenuate this noise and other high frequencies effectively, a third order low pass Chebyshev filter with a cutoff of 3.58MHz is constructed around the last NE5539 (Figure 2). This increases the S/N ratio significantly. Comparison photos taken from a spectrum analyzer are shown in Figure 3.

Caution should be exercised so as not to roll off too much of the 3.58MHz chrominance signal. A tradeoff between noise and color signal should be considered. Higher order filters using the NE5539 will sharpen the roll off considerably so that the color amplitude will not be affected. A comparison of input and output using the EIA color bar test signal is shown in Figure 4. As can be seen, there is excellent reproduction of the original signal and little overall phase shift in the vector plot. Also, using a 5 step staircase signal, differential gain and phase error measurements of the entire system are 1% and 0.5° respectively.

SYNOPSIS

The main intent is to show how to build a color video transmission system. But it may be possible to transmit other analog or digital signals along with the video since the circuit shown only utilizes the 20 to 40MHz band. These signals can be sent using the lower frequencies (i.e., data via FSK, voice channels, etc.). Additional circuitry can be used to multiplex the signals electronically after the first PLL, and bandpass filters utilized before the second PLL, on the receiver side, to separate and then demodulate them.

The circuit in Figure 1 can be made very inexpensively. The tools and connectors as well as instructions for constructing a very reliable fiber link are from Amp Inc. kit number 227385. The fiber used is ITT number T-3000, and the IR LED and photodiode are Motorola part numbers MFOE1202 and MFOD1100 respectively.

The circuits should be laid out on a double sided copper clad PC board with all power supply pins decoupled as shown. Care should be exercised in shielding both the PIN photodiode and the first NE5539 in the receiver end to avoid pick up and amplification of unwanted noise. The RF chokes are Ferroxcube part number VK200-10-3B. The I.C.'s are all available from Signetics.

Written by: Thomas DeLurio

Wideband FM Composite Video Fiber Optic Link

AN146

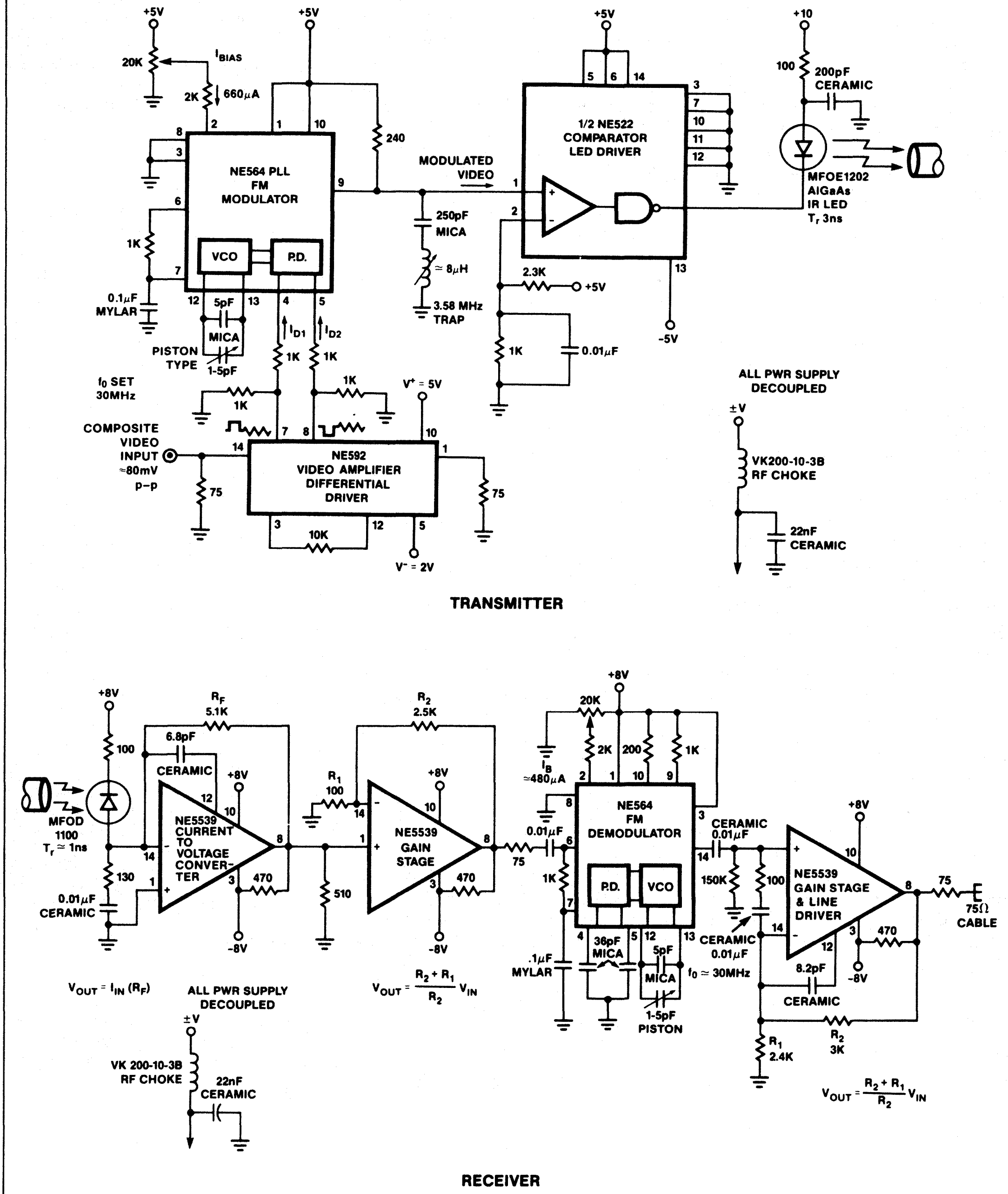


Figure 1. Fiber Optic Video System

Wideband FM Composite Video Fiber Optic Link AN146

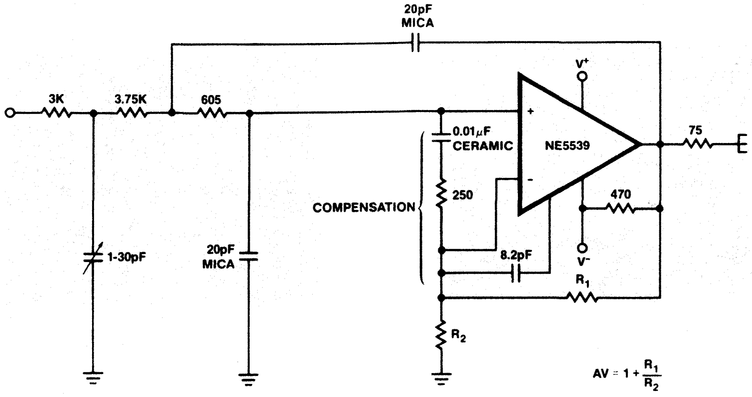
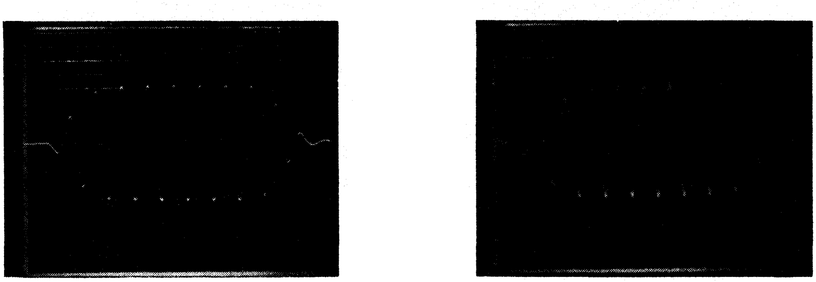
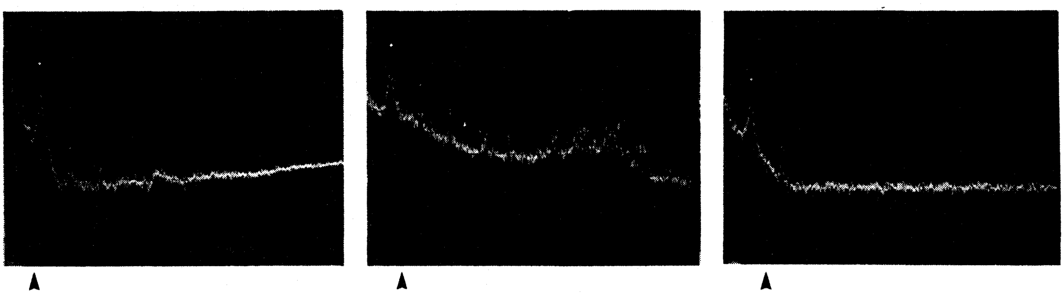


Figure 2. NE5539 CHEBYSHEV Low Pass Filter—3.58MHz Cutoff



INPUT 3.58MHz BURST

OUTPUT 3.58MHz BURST AFTER LOW PASS FILTER



3.58MHz

INPUT SIGNAL SPECTRUM 0 TO 40MHz

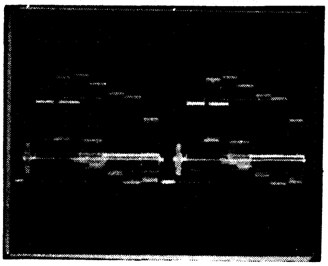
3.58MHz

OUTPUT BEFORE FILTER

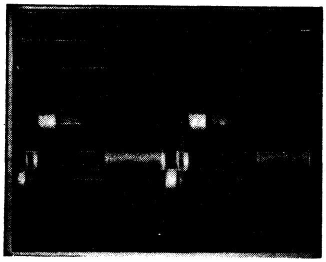
3.58MHz

OUTPUT AFTER FILTER

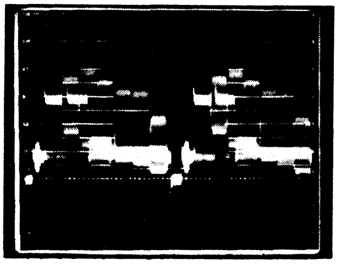
Figure 3. Noise Tests



INPUT



OUTPUT



OUTPUT AFTER FILTER

INPUT/OUTPUT VECTORS AFTER FILTER

Figure 4. Input/Output Test Signals Not to Scale

Progress in SMPS Magnetic Component Optimization

AN125

L. P. M. BRACKE

The last ten years have seen considerable progress in the development of the switched-mode power supply. Both design methods and associated hardware have been refined by experience and intensive development. These improvements, especially in the understanding of the influence of magnetic material and winding-conductor properties on SMPS operation, are reflected in the more straightforward and complete design routines now available. The better understanding that made for the improved design routines has also resulted in improved core designs: the ETD range of ferrite cores. Furthermore, lessons learned from experience in wound-component production have been applied to the design of the associated hardware, especially the coil former. The improved core and coil former, together with specially-developed assembly hardware, form the ETD system.

IMPROVED DESIGN ROUTINES

References 1 to 4 form a series of publications that presents complete design routines for the magnetic components of all common versions of SMPS. Part 1 of the Series (Ref.1) covers most aspects of SMPS design, with emphasis on the interaction between the electronic and magnetic aspects. The basic electrical relationships are given for forward, push-pull and flyback converters. Practical formulae are given for inductance and effective-current values. Auxiliary outputs and other special features are included in the coverage, as are related control aspects. All treatments are related to the magnetic design.

The data derived from Ref.1 are used in Part 2 of the Series (Ref.2) to select a suitable ferrite core for the transformer. Here, the magnetic and thermal properties of ferrite cores are considered as they affect their suitability for a given application. Initial selection of a suitable core is by means of charts showing the limits of performance to be expected at various frequencies. The optimum working conditions for cores in various transformer types are discussed, and a further chart enables this optimum to be determined. Wound transformer thermal characteristics are discussed, and formulae given for the losses in the core itself. Together with expressions for the number of turns required, Ref.2 allows the design of an SMPS transformer to progress from the electrical requirements set forth in Ref.1 to the mechanical design of the windings themselves discussed in Ref.3.

SELECTING THE CORRECT CORE

Most SMPS requirements can be satisfied by the range of cores currently available (Ref.5). The preferred grade of material for such high-frequency power applications is Ferroxcube 3C8.

Core selection charts

Due to the wide variation in application conditions, the selection charts have been designed to indicate the range of operation of the cores. This is done by using areas of throughput power as a function of frequency as shown in Fig.1. These are effectively areas of good design, since both boundaries represent the performance of a well-designed transformer.

The upper boundary of each area corresponds to a transformer design operating at optimum flux density sweep, with maximum use of the winding window, and Litz-wire windings, for minimum a.c. resistance. The lower boundary corresponds to a transformer design that also operates at optimum flux density, but has optimised solid-wire windings incorporating 8 mm creepage distance for IEC 435 mains isolation, and with a demagnetising winding occupying one third of the winding space.

Selection charts are given for push-pull, forward and flyback converter SMPS. However, the flyback converter charts are mainly intended as a cross-check on the design obtained by the method given in Ref.4 for chokes.

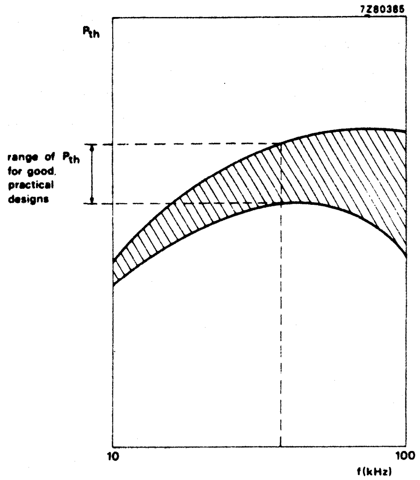


Fig.1 In the core selection charts given in Part 2 of the SMPS transformer design series (Ref.2), the power-handling capability of each core is plotted as a shaded area extending from 10 kHz to 100 kHz. The vertical boundaries of this area are the upper and lower limits of throughput power capacity achievable by good design but depending on conductor type and insulation requirements

Operating conditions

Converter type has the largest influence on throughput power obtainable, but other factors also influence performance, principally

- flux-density sweep
- winding configuration (simple or split, for example) and
- the presence of sensor or demagnetising windings
- the type of conductor used in the windings
- the number of output windings required
- mains insulation requirements.

Generally, the selection charts assume worst-case conditions. Operation at ambient temperatures lower than the 60 °C assumed, the use of feed-forward to ease the restriction on peak flux density (1/1.72 of saturation to allow for transient conditions), or heatsinking or potting to reduce thermal resistance, will all increase transformer power capacity.

Flyback transformers and chokes

Flyback converter transformers and output chokes are magnetically much the same: the main design requirement is stored energy, $\frac{1}{2}I^2L$. This is the basis of a separate design routine that includes winding design (Ref.4). This routine, using specially-developed design charts, leads directly to spacer thickness and number of turns.

OPERATING FLUX DENSITY

For chokes and flyback-converter transformers (which operate as chokes), stored energy is the basis of the design (subject to the core not being driven into saturation). With forward and push-pull converter transformers, the operating flux density (both a.c. and d.c. components) is set at the beginning of the design process.

Forward and push-pull converters

The operating flux density in forward and push-pull converter transformers strongly influences the overall volume of the transformer. Thus, it is set at the beginning of the design process to as high a level as practicable. For forward converter transformers, this level is determined by transient protection requirements or permissible core loss only. With push-pull converters, however, considerations of symmetry may dominate the choice.

Both forward and push-pull converter transformers must be designed to accommodate rapid changes of load. This is done by introducing a transient factor, usual symbol α, related to the range of input voltage for which the power supply is designed. A common value of α is 1.72. This is suitable for mains-fed supplies (215 V to 370 V or 200 V to 340 V), telephone supplies (40 V to 70 V), and mobile supplies (9 V to 15.5 V).

Considerations of symmetry usually result in the value of α being multiplied by a further factor ϵ for push-pull converter transformers. Asymmetry leads to core saturation, which in turn results in destruction of power switches. Principal causes of asymmetry are unbalanced flux linkage in windings (Ref.3) and unequal conduction times in switches. Where care has been taken to achieve balanced transformer windings, and protection circuitry is incorporated to ensure equal conduction times, the value of ϵ may be 1.15; that is, α is increased from 1.72 to 2 for a typical core. Where unbalance is accepted, however, the value of ϵ should be 2. (A list of the symbols used in this article, together with their definitions, is given as Table 1).

The use of feedforward (Ref.1) can considerably reduce the value of α required but at the expense of reduced transient response.

In forward-converter transformers core remanence should also be taken into consideration. However, the introduction of a small airgap in the core, and the use of a slow-rise capacitor (Ref.1) allows the whole first quadrant of the core hysteresis loop to be used.

TABLE 1
List of symbols

symbol	unit	definition
B_{ac}	T	flux-density sweep; half the peak-to-peak flux density excursion
B_{CF}	mm	coil former breadth
f	Hz	operating frequency
f_1	Hz	the frequency at which the number of turns on the lowest-voltage transformer winding becomes unity
f_L	Hz	the lowest frequency at which the coil former height is sufficient to accommodate ideal (minimum-loss) windings
f_T	Hz	the frequency above which no useful increase in the throughput-power capacity of a transformer can be obtained
H_{CF}	mm	coil former height
L	H	choke inductance
ℓ_{av}	mm	average turn length
P_c	W	total transformer core loss
$R_{th\,c}$	K/W	transformer or choke thermal resistance with winding creepage distance incorporated
$R_{th\,n}$	K/W	transformer or choke thermal resistance for a winding without creepage distance
V_e	m^3	effective volume of a core
α	–	ratio of core saturation flux to working flux allowed: for transient response without saturation
ΔT	K	temperature rise above ambient
ϵ	–	unbalance factor

subscripts

e	effective value
cp	pertains to centre pole

Figure 2 shows the maximum transformer flux-density sweeps for various converter types, and Table 2 gives the value of transient factors α and ϵ under various conditions.

Optimum flux-density sweeps

Manipulation of the expression (Ref.6) for the throughput power of an SMPS transformer shows that power reaches a maximum at a combination of operating frequency and flux density such that core loss is 44% of total loss. That is, when

$$0.44\ \frac{\Delta T}{R_{th}} = 16.7\ f^{1.3}\ B^{2.5}_{ac\,em}\ V_e$$

Here, the right-hand part of the expression is the typical hysteresis loss of Ferroxcube 3C8 ferrite. Since eddy-current loss is neglected, this expression applies only up to about 100kHz.

TABLE 2
Maximum values of flux-density sweep for various converter types and control circuits

boundary conditions	flux-density sweep $B_{ac\,cp}$ (T) forward	push-pull
maximum sweep for FXC 3C8 (100 °C)	0.16	0.32
at transient factor α	$\frac{0.32}{2\alpha}$	$\frac{0.32}{\alpha}$
with unbalance factor ϵ*	–	$\frac{0.32}{\epsilon\alpha}$
with x% feedforward	$\frac{0.32}{2\,(1 + x/100)}$	$\frac{0.32}{(1 + x/100)}$
with unbalance factor ϵ and x% feedforward	–	$\frac{0.32}{\epsilon\,(1 + x/100)}$

* ϵ is the ratio of peak flux density in a balanced converter to the peak flux density in an unbalanced converter.

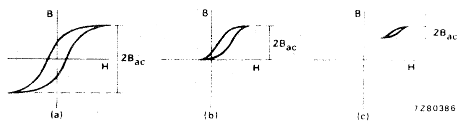


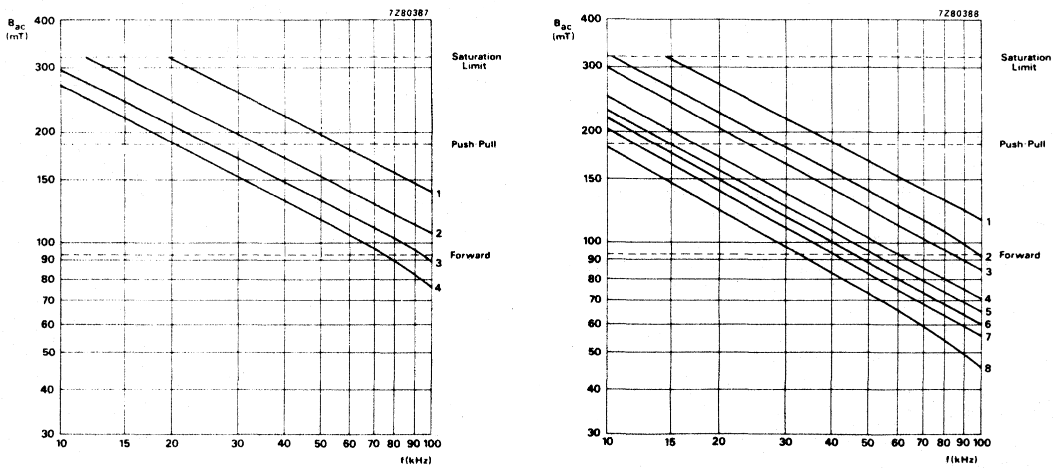
Fig.2 Flux-density excursions and corresponding flux-density sweeps for (a) push-pull, (b) forward converter transformers (with slow-rise capacitor) or ringing choke, and (c) flyback converter chokes

Using this expression, curves of $B_{ac\,em}$, the peak flux-density sweep, have been derived for all Philips' SMPS transformer cores (See Fig.3).

THERMAL RESISTANCE AND TEMPERATURE RISE

The maximum permissible dissipation of a transformer or choke is set by its maximum operating temperature; ambient temperature and thermal resistance depend on core size, mounting method and attitude, the type of conductor in the winding and the amount of insulation incorporated. Due to the insulating effect of the interleaving where 8 mm creepage distance is allowed for in the windings, two values are quoted for thermal resistance in Ref.2: with and without creepage allowance.

Measurement methods are discussed in Ref.2 and 7. Results given in Ref.7 confirm that transformer temperature rise can be accurately calculated from the product of total transformer dissipation and thermal resistance for any ratio of core to winding loss.



1 UU15/22/6 EE20/20/5 2 UU20/32/7 EE25/25/7 EE30/30/7
3 UU25/40/13 4 UU30/50/16

1. EC 35 2. EC41, EC52 3. EC70 4. EE42/42/15
5. EE42/42/20. EE42/54/20 EE42/66/20 6. EE55/55/21
7. EE55/55/25. UU64/79/20 8. EE65/66/27

Fig.3 Optimum, peak, centre-pole flux-density sweeps $B_{ac\,cp}$ for a variety of cores for SMPS applications. Horizontal lines indicate the limits for various converter types ($\alpha = 1.72$). The curves were calculated for a peak temperature rise of 40 K

THE EFFECT OF OPERATING FREQUENCY

Winding properties

Depending on frequency, the windings of an SMPS transformer fall into one of three categories. At low frequencies, the available winding-window height will be insufficient to accommodate minimum-loss (ideal) windings. At some higher frequency, f_L, the height of minimum-loss windings becomes less than that of the winding window. Finally, at some higher frequency, f_1, the number of turns required for the lowest-voltage winding becomes unity.

It is shown in Ref.8 that, where the winding height is insufficient for minimum-loss windings, winding loss is inversely proportional to the squares of both flux-density sweep and operating frequency. At frequencies above f_L winding loss becomes inversely proportional to operating frequency.

Flux density sweep

From the considerations given earlier, it is apparent that at lower frequencies, operating flux density is limited by core saturation rather than loss. Above some frequency f_T, the optimum operating flux density (for maximum power) becomes less than the saturation-related maximum, and the flux-density sweep is limited by the requirement that (for Ferroxcube 3C8) core loss $P_c = 0.44\,P_{tot}$, where P_{tot} is the total permissible dissipation.

Throughput power

In Ref.8, these various effects of operating frequency are combined to explain the observed variation of SMPS transformer throughput power with operating frequency for Ferroxcube 3C8 cores. Figure 4(a) shows the division between core and winding loss for an SMPS transformer as a function of operating frequency. Frequencies f_L, f_T and f_1, are marked. (Note that f_L may, in fact, be higher than f_T for some cores. This does not alter the main argument.) In Region I, operating flux density is limited by saturation considerations only, so that throughput power is roughly proportional to frequency. Operation remains saturation limited into Region II, but here power increases roughly as the root of the frequency. (This relationship is complicated by the fact that average turn length decreases as ideal-winding height decreases.) Region III begins at f_T, where core operating flux density becomes limited by core loss to the optimum value for that frequency. The shape of the throughput power curve in the region depends on core material characteristics: the Steinmetz coefficient and its associated flux-density and frequency exponents. For Ferroxcube 3C8, flux density is inversely proportional to the root of frequency. Then, winding resistance decreases slightly with frequency so that, since winding loss is constant, throughput power is also about constant.

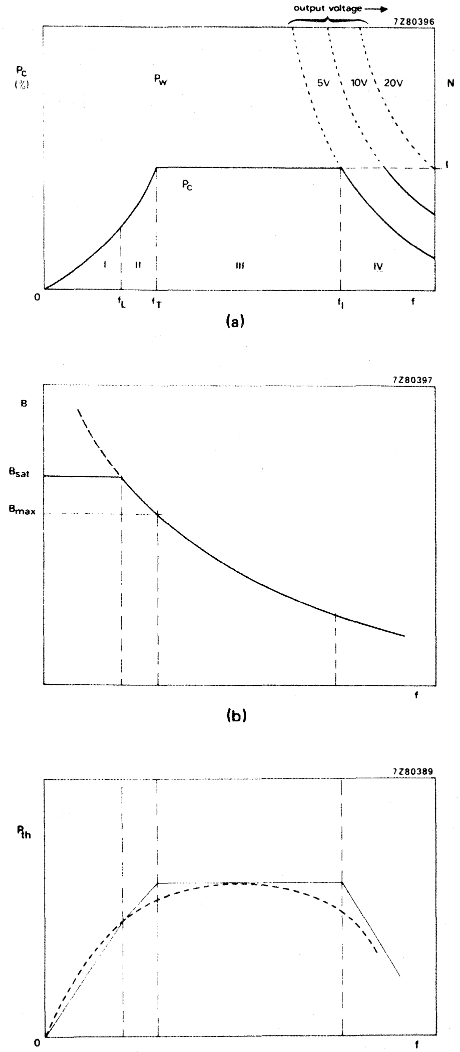


Fig.4 (a) Division of transformer loss between core loss and winding loss as a function of frequency, showing the various boundary frequencies. (b) Relation between flux density and frequency for maximum throughput power. (c) The corresponding throughput power characteristic

Region IV begins where frequency increases to the point where the number of turns required on the lowest-voltage winding falls to unity. (Contours of number of turns N as a function of frequency for various voltages are indicated in Fig.4(a)). When this happens, flux density must then decrease with frequency. The rate of this decrease is greater than that required for optimum core loss, so that throughput power decreases. The effect is accentuated by the increasing contribution of eddy-current losses at high frequencies.

In practice, other factors, such as eddy-currents, parasitic capacitance and rounding of numbers of turns, cause the transitions from one Region to another to become blurred so that, as Fig.4(c) shows, the thoughput power characteristic is more rounded. Calculated values for real cores, Fig.5, shows that the general characteristics remain, however: there is always a frequency, close to the core transition frequency, above which no useful increase in throughput power can be obtained.

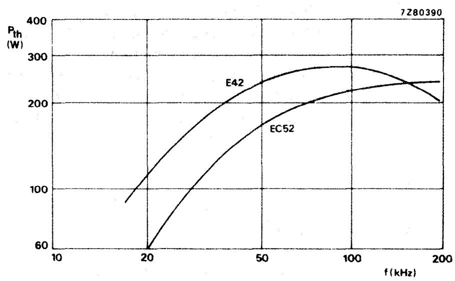


Fig.5 Calculated throughput powers (5 V forward converters) with frequency for EC52 and E42/21/20 core show the same general characteristics: there is a frequency (from Fig.3) above which no useful increase in throughput power can be obtained. For the EC52 core this is 100 kHz, for the E42 core it is 52 kHz

EFFECT OF CORE DESIGN

The more complete understanding of the factors that influence throughput power obtainable has made it possible to examine established core designs with a view to improving the designs available. Electrical, magnetic and mechanical considerations can now be combined so that the core can be made as effective as possible.

Existing core designs

Analysis of existing core designs (E, EC, PM, PQ and RM cores, Ref.8) shows that performance agrees well with values of f_T. The performance of the smaller cores is found to be relatively poor at 50 kHz due to lack of sufficient winding-window height for ideal windings.

The effectiveness of the use of core materials is another important consideration, since it directly affects the weight of an SMPS. Constant cross-section E cores generally have the best power-to-weight ratios.

Progress in SMPS Magnetic Component Optimization

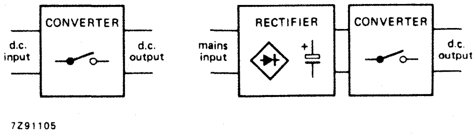
AN125

SWITCHED-MODE POWER SUPPLIES

The essential difference between switched-mode and conventional (mains) power supplies is operating frequency. Whereas conventional power supplies operate at mains frequencies, 50 Hz or 60 Hz, switched-mode power supplies (SMPS) operate at frequencies of the order of 50 kHz. The complications associated with operation at these high frequencies are more than compensated for by the savings in weight and volume, especially of transformers and smoothing components.

Voltage conversion and control in SMPS is achieved by chopping the incoming supply voltage with a high-speed switch such as a transistor. The chopped voltage is applied to a transformer which performs voltage conversion and provides isolation. This transformer is generally wound on a ferrite core, and is much smaller and lighter than a 50 Hz unit of comparable power capacity. Fine control of output voltage is obtained by varying the duty cycle of the switch.

Most SMPS converters require a d.c. input and provide a d.c. output. For operation from the mains, therefore, a rectifier and smoothing circuit generally precedes the converter itself, Fig.A.

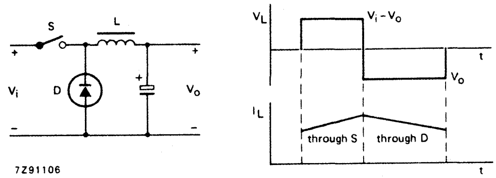


A

SMPS converters

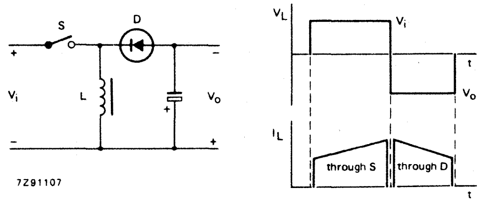
There are three basic SMPS converter arrangements; they and their variants are discussed in detail in Ref.1.

In the forward converter, Fig.B, power is transferred directly to the load while the switch is closed; the energy stored in the inductor is transferred to the load while the switch is open. The switch may be transformer coupled to the inductor for input/output isolation.



B

In the flyback converter, Fig.C, power is stored in the inductor while the switch is closed and transferred to the load while the switch is open. The functions of transformer and inductor may be combined where voltage transformation is required.



C

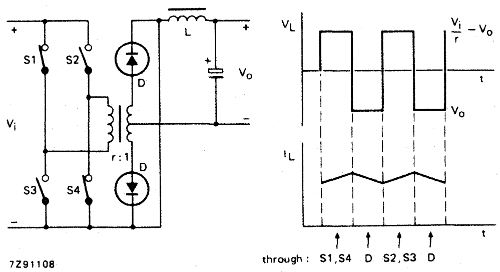
The push-pull converter is, effectively, a forward converter in which the output choke is driven by any push-pull arrangement of power transistors, including a full bridge, Fig.D. Operation after the transformer is similar to that of a forward converter, but with twice the effective switching frequency.

Transformer and choke requirements

There are two main boundary conditions for the power transformer: it must not saturate (otherwise the power transistors will be damaged) and it must not overheat. In addition to these boundary conditions, the output choke should be capable of storing sufficient energy to deliver one output cycle so that ripple will be low and regulation good.

Saturation is prevented by designing for worst probable combinations of load change and input voltage fluctuation. In forward converters, provision must be made for removing energy stored in the transformer at the end of the ON period of the switch. In push-pull converters, the degree of symmetry achievable in both power switches and transformer windings determines the unbalance allowance.

Overheating of the transformer and choke is prevented by calculation of total power dissipation: core hysteresis and eddy current losses, and winding losses.



D

Mechanical design is of great importance since this influences manufacturing cost and transformer production cost. The core should be cheap to manufacture. Enclosed cores, such as pot cores and their variants (RM, PQ, PM cores) are more expensive to make than E cores for a given power capacity. However, round centre legs make for easier winding, with less leakage inductance – especially for strip. For all but the smallest transformers, E cores result in more compact design than U cores. Finally, due to their symmetry, E cores require some 20% less core material for a given power capacity than U cores, with a consequent reduction in eddy-current losses. This last point is of especial importance at higher operating frequencies.

Core design requirements

From this theoretical and practical background the requirements for a new core design are clear. The range of cores should be optimised for frequencies appropriate to their power handling capacity: 50 kHz for 300 W, 100 kHz for 100 W, for example. This requires proper choice of f_L and f_T. Optimisation should be aimed at forward-converter applications (the cores will then also be suitable for unbalanced push-pull converters).

The design of the associated coil formers is also critically important. They should be suitable for automatic handling. A large number of pins is required, both for flexibility of layout and to accommodate multiple secondaries.

The core and wound coil former should be quick and easy to assemble. The combination should be designed for horizontal mounting on p.c. boards to minimise height and make termination of strip windings easier.

THE ETD SYSTEM

The cores

These criteria have been adopted in the design of the ETD cores (Ref.8). They are constant cross-section E cores in Ferroxcube 3C8 ferrite with round centre legs, photo and Fig.6, and are designed for

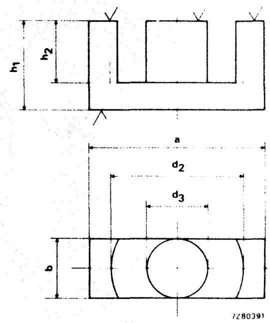
- minimum throughput powers in the range 100 W to 300 W
- economical manufacture
- minimum weight of ferrite
- operating frequencies in the range 50 kHz to 150 kHz
- high throughput power density
- mains isolation
- minimum transformer volume and p.c. board areas.

Magnetic properties are given in Table 3.

The ETD cores are compared with existing core designs for power per unit weight in Fig.7. Throughput power areas as a function of frequency for ETD cores are given in Fig.8, and the optimum flux density sweep in Fig.9.

TABLE 3
Magnetic dimensions of ETD system cores

core type	$A_{cp\,min}$ (mm²)	A_e (mm²)	V_e (mm³)	ℓ_e (mm)
ETD 34	87	97.1	7 640	78.6
ETD 39	117	125	11 500	92.2
ETD 44	167	173	17 800	103
ETD 49	204	211	24 000	114



core type	mid-limit dimensions (mm) a	d_2	d_3	h_1	h_2	b	mass (g) (core half)
ETD 34	34.2	26.3	10.8	17.3	12.1	10.8	20
ETD 39	39.1	30.1	12.5	19.8	14.6	12.5	30
ETD 44	44.0	33.3	14.9	22.3	16.5	14.9	47
ETD 49	48.7	37.0	16.4	24.7	18.1	16.4	62

Fig.6 Outline drawing and dimensions of the new ETD core range

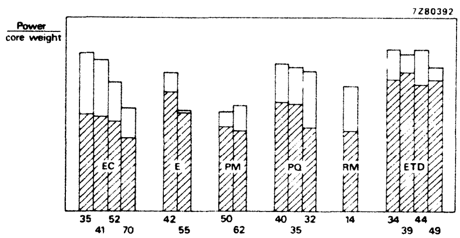
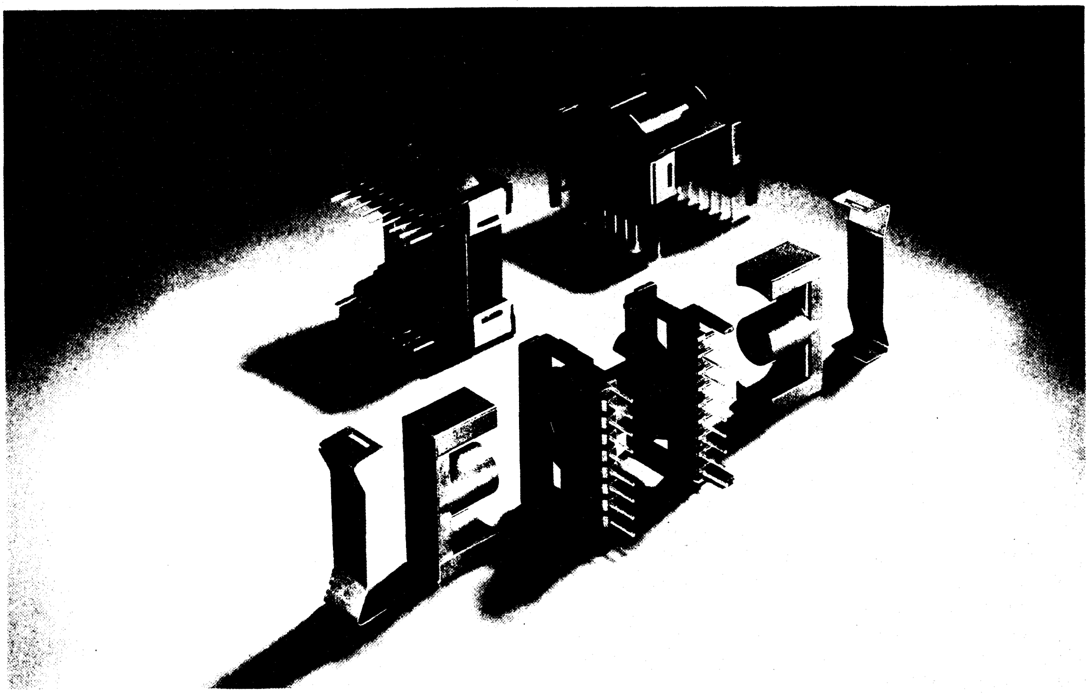


Fig.7 The throughput power per unit weight of core material for ETD cores compared with that of other popular core types at two operating frequencies: 50 kHz (shaded areas) and 100 kHz (open areas). Forward-converter operation is assumed

8



These ETD system components provide OEMs with the most efficient and economical route to SMPS transformers

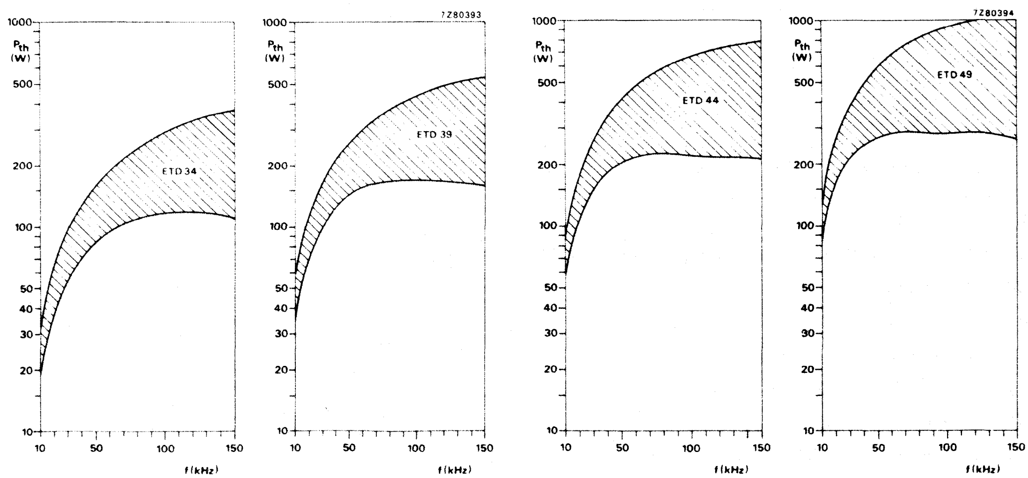


Fig.8 Throughput power as a function of frequency for ETD cores in forward-converter transformers

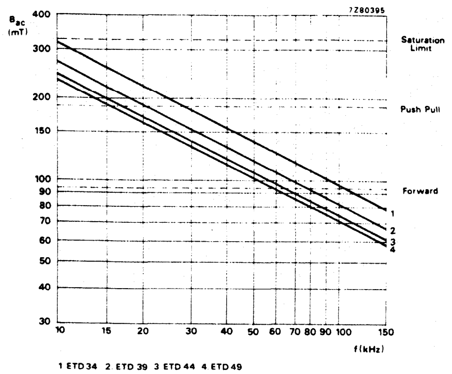


Fig.9 Optimum flux-density sweeps for ETD cores

The coil former and assembly hardware

Simple, rapid winding and assembly of ETD-system based transformers and chokes is made possible by the coil former of Fig.10, together with the associated snap-on stainless-steel assembly clips.

Principal features of the design are indicated in Fig.10:

– the length and number of slots gives a wide choice of lead-out position

– there is at least 8 mm creepage distance from the pins to the ferrite core

– the pegs between the slots allow wire to be run from any one slot or pin to any other

– the four support legs provide 8 mm creepage distance between the windings and the p.c. board

– the hood over the pins provides 8 mm creepage distance between leadouts and assembly clips

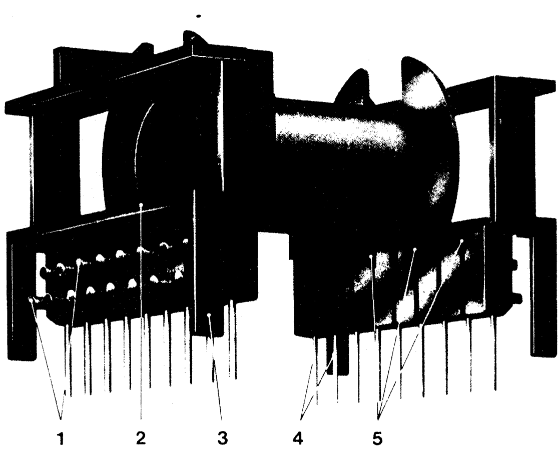
– a separate earthing clip for the core is to be available.

The coil former itself is moulded in polybutylene terephthalate, a high-grade, flame retardant (UL 94-VO), thermoplastic. Windings dimensions are given in Table 4.

TABLE 4
Winding dimensions of ETD-system coil formers

type	B_{CF} (mm)	H_{CF} (mm)	ℓ_{av} (mm)
ETD 34	20.9	5.9	61
ETD 39	25.7	6.9	69
ETD 44	29.5	7.3	78
ETD 49	32.7	8.4	86

ETD system components provide OEMs with the most efficient electrical, magnetic and mechanical route to full, economical, automated production of SMPS transformers.



1 – pegs allow wires to be taken from most appropriate slot to chosen pin
2 – these plates give 8 mm creepage distance between wires and assembly clips
3 – legs give 8 mm creepage distance from windings and p.c. board.
4 – 8 mm creepage from pins to core
5 – multiple slots for maximum freedom of lead-out position

Fig.10 Coil former design for the ETD system, intended for automatic winding

8

REFERENCES

1. Bracke, L. P. M. and Geerlings, F. C. 1982. High-frequency ferrite power transformer and choke design. Part 1: Switched-mode power supply magnetic component requirements. Philips' ordering code: 9398 923 20011.
2. Bracke, L. P. M. 1982. High-frequency ferrite power transformer and choke design. Part 2: Switched-mode power supply magnetic considerations and core selection. Philips' ordering code: 9398 923 30011.
3. Jongsma J. 1982. High-frequency ferrite power transformer and choke design. Part 3: Transformer winding design. Philips' ordering code: 9398 923 40011.
4. Bracke, L. P. M. and Jongsma, J. 1982. High-frequency ferrite power transformer and choke design. Part 4: Improved method of power-choke design. Philips' ordering code 9398 923 50011.
5. Philips' Data Handbook, Vol. C5. Ordering code 9398 923 50011.
6. Jansson, L. E. 1976. Power capacity of ferrite-cored transformers and chokes in switched-mode power supplies. E.A.B. 34, 20-47 (No. 1).
7. Bracke, L. P. M. 1982. Optimizing the power density of ferrite-cored transformers. Proc. PCI/Motorcon, Geneva. Intertech Communications, Inc., Oxnard, California.
8. Bracke, L. P. M. 1982. Optimizing the configuration of ferrite-cored transformers for advanced switched-mode magnetics, Proc. Powercon 9, Washington. Power Concepts, Inc., Ventura, California.

SO Package Tape and Reel | AN210

Integrated Circuits packaged and shipped in Tape and Reel will significantly alter the production methods of the US electronics industry. SO packages are now available in 12mm, 16mm, and 24mm tapes depending on the size of the package.

Tape and Reel will enable manufacturers to use very high speed automatic placement equipment. With reels containing 1000 or 2000 components each, this equipment can run at high speed for longer periods without stopping the machine to replace empty tubes. Further, the components packaged in Tape and Reel require much less storage space than those in the traditional tubes. For example, the SMD Technology Center in Milwaukee, WI saved over 90% in storage area for 5,000,000 SMDs in Tape and Reel vs. the space it would have required for the traditional axial leaded parts in tubes and/or reels.

Table 1.

PACKAGE TYPE	TAPE WIDTH	TAPE PITCH	PARTS PER REEL	REEL DIAMETER	REEL WIDTH
SO-8	12mm	8mm	2000	330mm	18.4mm
SO-14	16mm	8mm	2000	330mm	22.4mm
SO-16	16mm	8mm	2000	330mm	22.4mm
SO-16L	24mm	12mm	1000	330mm	22.4mm
SO-20	24mm	12mm	1000	330mm	30.4mm
SO-24	24mm	12mm	1000	330mm	30.4mm
SO-28	24mm	12mm	1000	330mm	30.4mm

Table 2. SURFACE RESISTIVITY

ITEM	RESISTIVITY RANGE	RESISTIVITY VALUES	SPECIFICATION
Carrier Tape	CONDUCTIVE	$<1 \times 10^5 \Omega/sq$	$<1 \times 10^5 \Omega/sq$
Cover Tape	ANTISTATIC	$>10^9$ to $>10^{14} \Omega/sq$	None
Reel	ANTISTATIC	$>10^9$ to $>10^{14} \Omega/sq$	None

SPECIFICATIONS

Tape and Reel specifications conform to Electronic Industries Association (EIA) Proposed Specification #RS-481 A, "Taping of Surface Mounted Components for Automated Placement".

The carrier tape material is PVC with a carbon filler and the cover tape is polyester. The reel material is cardboard.

Signetics' SO packages will be loaded onto reels in the quantities indicated in Table 1.

Components packaged in Tape and Reel are protected against damage due to electrostatic discharge. The carrier tape is conductive, as shown in Table 2. Resistivity measurements are in accordance with ASTM-D-991.

The cover tape is heat sealed to the carrier tape along the outer edges of the cover tape. The seal releases when pulled with a peelback force (Z) of 15 grams (min.) to 65 grams (max.). The peelback force must be exerted at an angle of 180-175° with respect to the carrier tape direction. Peel speed is 120±5mm/min.

Components are loaded with pin #1 on the side nearest the sprocket holes. The carrier tape, cover tape, and reels are designed to withstand normal conditions seen in the industrial environment without changes in dimensions or other physical properties. COMPONENTS ARE FULLY PROTECTED FROM LEAD DAMAGE ONCE THEY ARE LOADED INTO THE TAPE.

BOXES

Taped components will be shipped in foil lined packing boxes approximately 16″ × 16″ × 1½″ which will in turn be placed in shipping boxes that are 16″ × 16″ × 10″. The shipping boxes can hold up to 5 packing boxes.

ORDERING

To order Tape and Reel, simply indicate with the letter 'R' after the part number (example: N74LS00DR). This SPC code identifies to the factory that this is a Tape and Reel order. Orders for Tape and Reel MUST BE FOR WHOLE REELS, i.e. 2000 units of SO-8, SO-14 and SO-16, and 1000 units of SO-16L, SO-20, SO-24 and SO-28. NO PARTIAL REELS WILL BE SHIPPED.

SAMPLES

Full reels of dummy parts will be available through Logic Division for purchase by customers who would like to use dummies to check out their automatic pick-and-place machines.

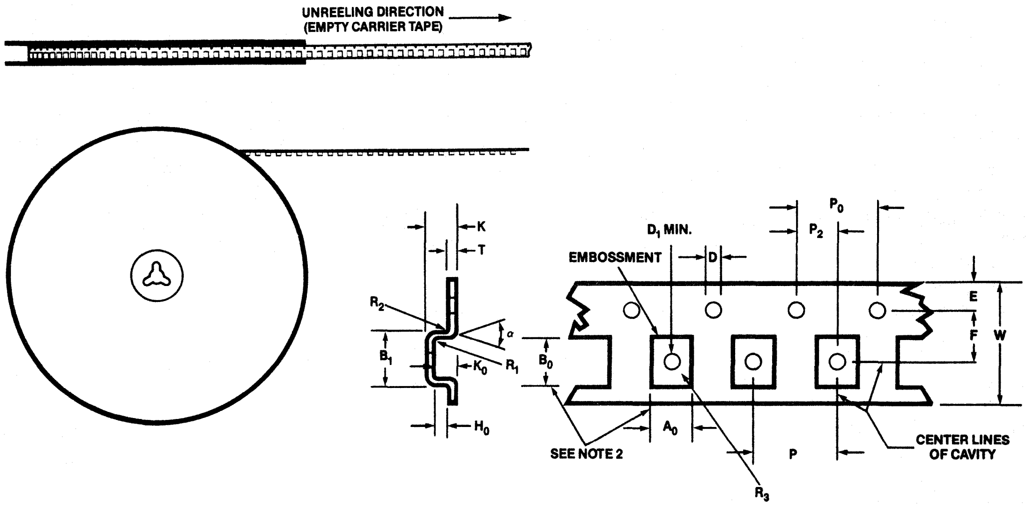
To Get...	Order...
DUMMY-SO-8	M1511DE R
DUMMY-SO-14	M1511DH R
DUMMY-SO-16	M1511DJ R
DUMMY-SO-16L	M1511DJA R
DUMMY-SO-20	M1511DLA R
DUMMY-SO-24	M1511DNA R
DUMMY-SO-28	M1511DQA R

Written by: Mark Kastner

8

SO Package Tape and Reel

AN210



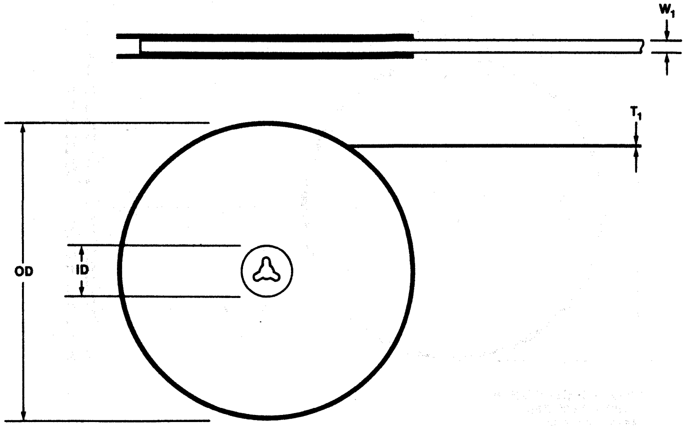
ITEM		FOR ALL COMPONENTS			VALUE BY COMPONENT						
		SYMBOL	SPECIFICATIONS Value	Tolerance	SO-8	SO-14	SO-16	SO-16L	SO-20L	SO-24L	SO-28L
Carrier Tape	Width	W		±0.30	12	16	16	16	24	24	24
	Film Thickness	t	0.40	Max.							
	Total Thickness	K		Max.	2.4	2.4	2.4	3.2	3.2	3.2	3.2
	Camber	δ	0.3	Max.							
Compartments	Length, Inside	A_0		±0.1	6.33	6.35	6.35	10.8	10.8	10.8	10.8
	Width, Inside	B_0		±0.1	5.15	8.90	10.15	10.65	13.15	15.75	18.25
	Depth, Inside	K_0		±0.1	1.9	1.9	1.9	2.80	2.80	2.80	2.80
	Width, Outside	B_1		Max.	8.2	12.1	12.1	12.1	20.1	20.1	20.1
	Length, Outside										
	Depth, Outside										
	Radius	R_1, R_2, R_3	0.3	Max.							
	Pitch	P		±0.1	8	8	8	12	12	12	12
	Wall Angle	α	6°	±1.0							
	Ref. Plane	H_0	0.3	+0.10 – 0.05							
	Center Line Distance, Width	P_2	2.0	±0.05	Compartment to Sprocket Hole						
	Center Line Distance, Length	F		±0.05	5.5	7.5	7.5	7.5	11.5	11.5	11.5
	Hole Diameter	D_1	1.5	Min. ⊕|ϕ0.2							
Sprocket Hole	Diameter	D	1.55	±0.05							
	Pitch	P_0	4.0	±0.1							
	10-Pitch	—	40.0	±0.2							
	Distance to Edge	E	1.75	±0.1							

NOTES:
1. All feature dimensions in millimeters.
2. A_0 and B_0 dimensions are measured at a plane defined as H_0 distance up from the inside compartment bottom and parallel to the bottom. K_0 is measured from the same plane to the top surface of the tape.
3. Camber to be no more than 1.0mm per 250mm length measure per semi specification #G10-83-(Camber).
4. Pin #1 to be nearest sprocket holes. Top side of the package will be up.

Figure 1. Embossed Carrier Tape Specifications

SO Package Tape and Reel

AN210



ITEM		FOR ALL COMPONENTS			VALUE BY COMPONENT						
		SYMBOL	SPECIFICATIONS		SO-8	SO-14	SO-16				
			Value	Tolerance				SO-16	SO-20	SO-24	SO-28
Cover Tape	Width	W_1		−0.5	9.0	13.0	13.0	13.0	21.0	21.0	21.0
	Thickness	T_1	0.1	Max.							
	Break Force	—	1.0KG	Min.							

Figure 2. Cover Tape Specifications

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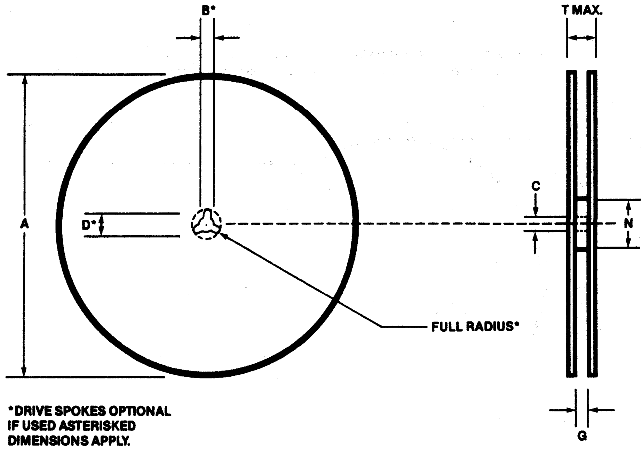


ITEM			FOR ALL COMPONENTS			VALUE BY COMPONENT						
			SYMBOL	SPECIFICATIONS		SO-8	SO-14	SO-16				
				Value	Tolerance				SO-16	SO-20	SO-24	SO-28
Reel Flange	Diameter, Outside		A	330	Max.							
	Thickness		t									
	Space Between Flanges		G		+2.0	12.4	16.4	16.4	16.4	24.4	24.4	24.4
Reel Hub	Diameter, Outside		N	55	±2.0							
	Diameter, Hole		C	13.0	±0.5							
	Key Slots	Width	B*	1.5	Min.							
		Diameter	D*	20.2	Min.							
		Location	o	120°								
Reel Assy.	Thickness		T		Max.	18.4	22.4	22.4	22.4	30.4	30.4	30.4

NOTES:
1. All feature dimensions in millimeters.
2. A clearance of 0.1mm to 2.2mm max. will be maintained between the carrier tape and the reel at the hub. This clearance will be measured at the hub O.D.
3. Dimension T and G will be measured at the hub O.D.

Figure 3. Reel Specifications

Section 9
Package Outlines

INDEX

SECTION 9 – PACKAGE INFORMATION

PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

PLASTIC ONLY

5. Lead material: Alloy 42 (Nickel/Iron Alloy) Olin 194 (Copper Alloy) or equivalents, solder dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.
9. SO Packages-microminiature packages.
   a. Lead material: Alloy-42.
   b. Body material: Plastic (Epoxy).

HERMETIC ONLY

10. Lead material
    a. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
    b. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated, gold plated or solder dipped.
    c. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
11. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seal at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
12. Lid Material
    a. Nickel or tin plated nickel, weld seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold plated, alloy seal.
    d. BeO Ceramic with glass seal.
13. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
14. Recommended minimum offset before lead bend.
15. Maximum glass climb .010 inches.
16. Maximum glass climb or lid skew is .010 inches.
17. Typical four places.
18. Dimension also applies to seating plane.

PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

PLASTIC PACKAGES			
	PACKAGE CODE	θ_{ja}/θ_{jc}(°C/W)	DESCRIPTION
Standard Dual-in-Line Packages			
8-Pin	N	99/50	
14-Pin	N	86/48	TO-116/MO-001
16-Pin	N	83/42	MO-001
18-Pin	N	63/29	
20-Pin	N	61/24	
22-Pin	N	51/23	
24-Pin	N	52/23	MO-015
28-Pin	N	52/23	MO-015
Metal Headers			
4-Pin	E	100/20	TO-46 Header
4-Pin	E	150/25	TO-72 Header
8-Pin	H	150/25	TO-5 Header
10-Pin	H	150/25	TO 5/TO-100 Header, Short Can
10-Pin	H	150/25	TO-5/TO-100 Header, Tall Can
Cerdip Family			
8-Pin	FE	110/30	Dual-in-Line Ceramic
14-Pin	F	110/30	Dual-in-Line Ceramic
16-Pin	F	100/30	Dual-in-Line Ceramic
18-Pin	F	93/27	Dual-in-Line Ceramic
20-Pin	F	90/25	Dual-in-Line Ceramic
22-Pin	F	75/27	Dual-in-Line Ceramic
24-Pin	F	60/26	Dual-in-Line Ceramic
28-Pin	F	57/27	Dual-in-Line Ceramic
Laminated Ceramic, Side Brazed Lead			
16-Pin	I	90/25	Dip Laminate

SO Package Thermal Data

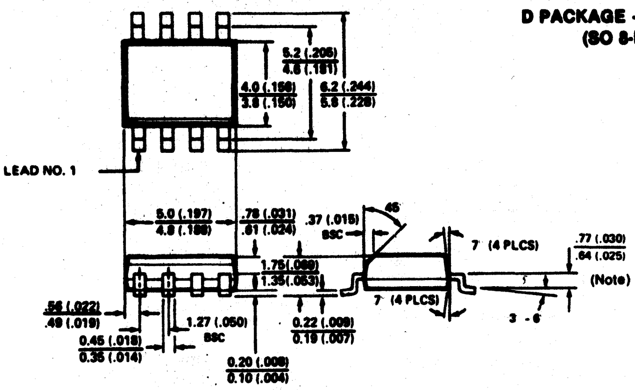
Package Type	Package Mounting Technique*	Max. Allowable Power Diss. (mW) at 25°C	Max. Allowable Power Diss. (mW) at 70°C	Thermal Resistance (θ_{JA}°C/Watt) Average	Thermal Resistance (θ_{JA}°C/Watt) Maximum
SO-14	PCB	658	421	190	225
	Ceramic	962	615	130	165
	Ceramic w/H.S.	1471	941	85	110
SO-16	PCB	862	551	145	170
	Ceramic	1250	800	100	125
	Ceramic w/H.S.	1923	1231	65	85
SO-16L	PCB	1250	800	100	140
	Ceramic	1743	1143	70	100
	Ceramic w/H.S.	2500	1600	50	65
SO-20	PCB	1471	941	85	115
	Ceramic	2273	1454	55	85
	Ceramic w/H.S.	3572	2286	35	55
SO-24	PCB	1563	1000	80	110
	Ceramic	2000	1600	50	80
	Ceramic w/H.S.	4167	2667	30	50

PCB = Printed circuit board
Ceramic = Ceramic substrate
Ceramic w/H.S. = Ceramic substrate with heat sink and/or thermal compound
*Air gap is 0.006 inches unless thermal compound is used

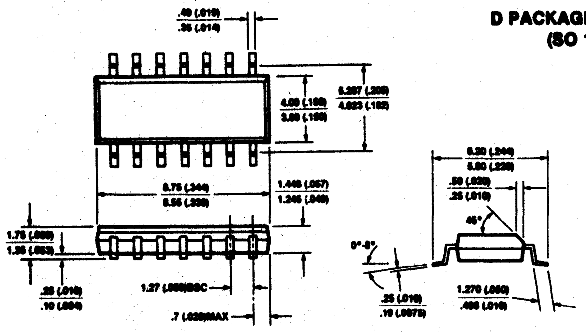
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

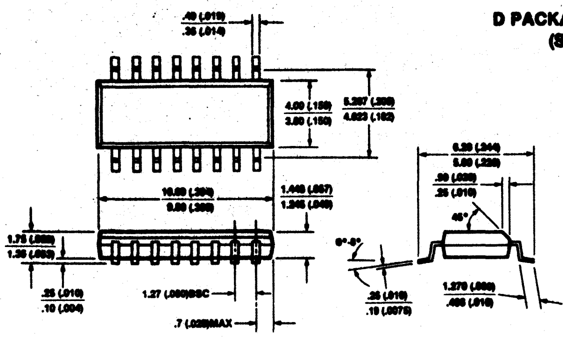
D PACKAGE — PLASTIC (SO 8-PIN)



D PACKAGE — PLASTIC (SO 14-PIN)



D PACKAGE — PLASTIC (SO 16-PIN)



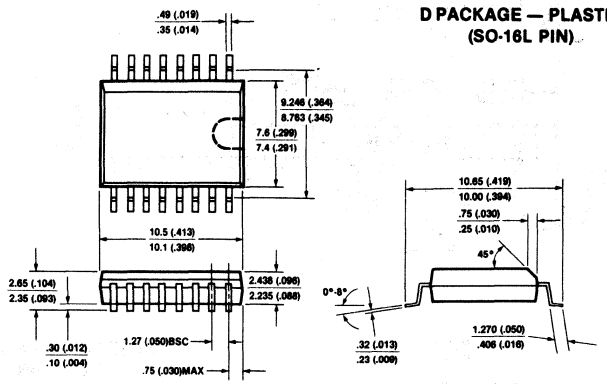
Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

9

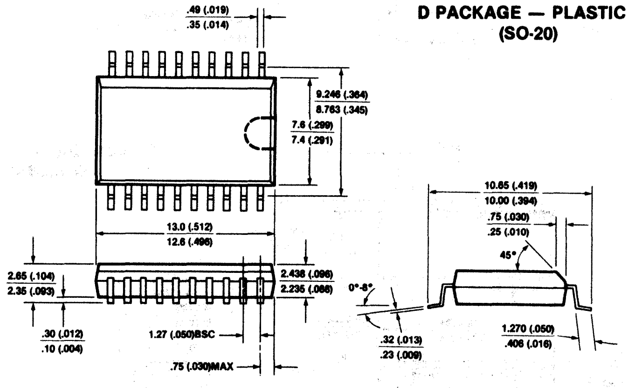
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

D PACKAGE — PLASTIC (SO-16L PIN)



D PACKAGE — PLASTIC (SO-20)

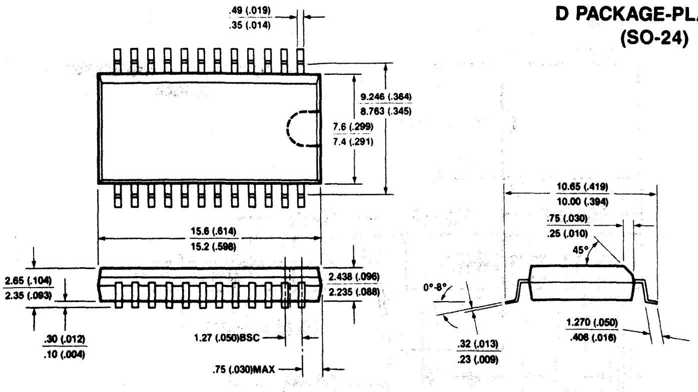


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

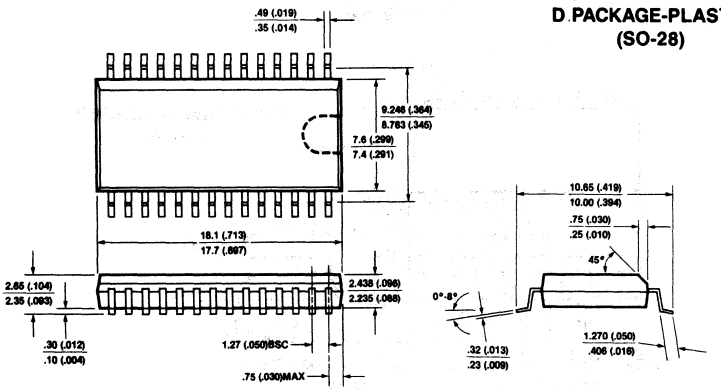
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

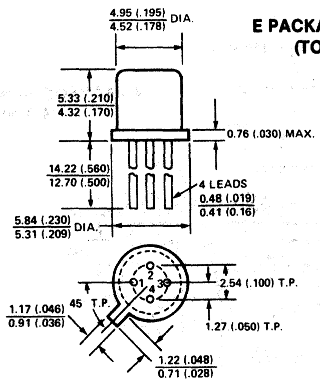
D PACKAGE-PLASTIC (SO-24)



D PACKAGE-PLASTIC (SO-28)



E PACKAGE — HERMETIC (TO-72 HEADER)



Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

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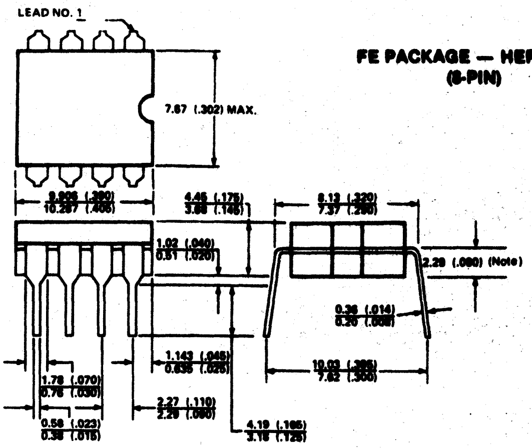
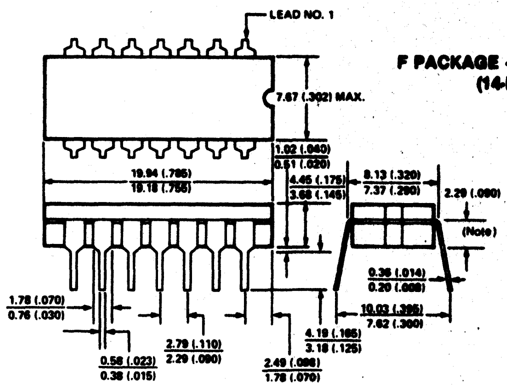
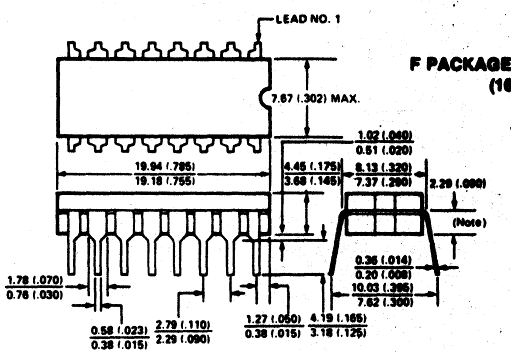
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN





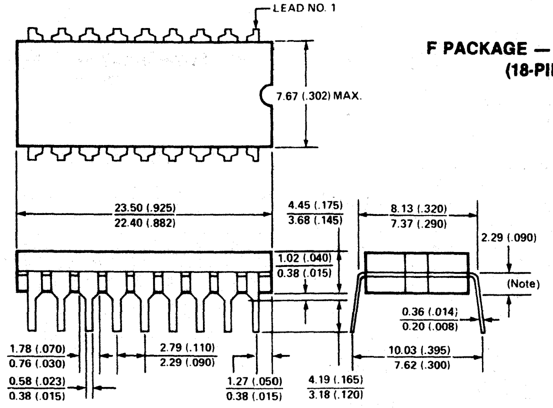


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

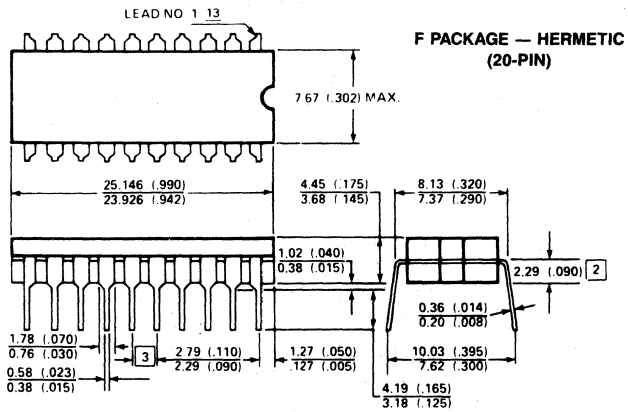
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

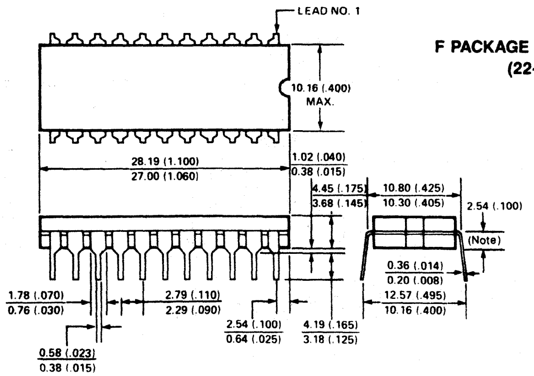
F PACKAGE — HERMETIC (18-PIN)



F PACKAGE — HERMETIC (20-PIN)



F PACKAGE — HERMETIC (22-PIN)

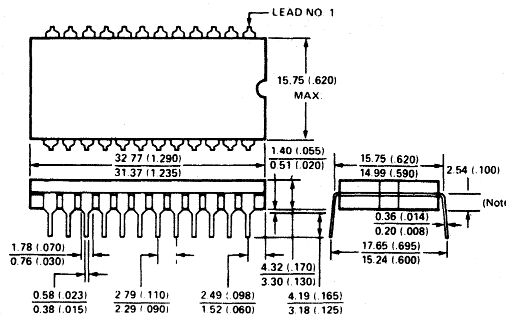


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

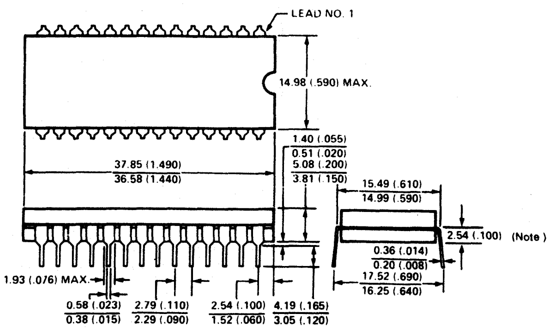
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

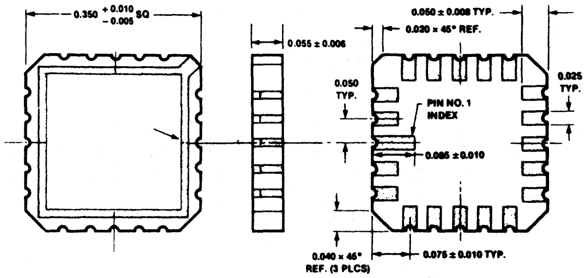
F PACKAGE — HERMETIC (24-PIN)



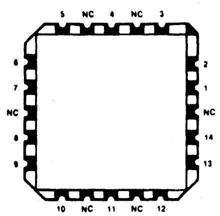
F PACKAGE — HERMETIC (28-PIN)



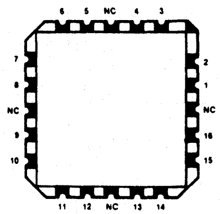
G PACKAGE



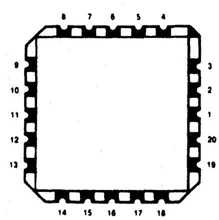
G PACKAGE (14-PIN)



G PACKAGE (16-PIN)



G PACKAGE (20-PIN)

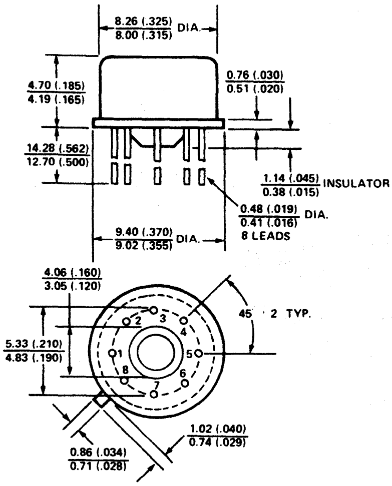


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

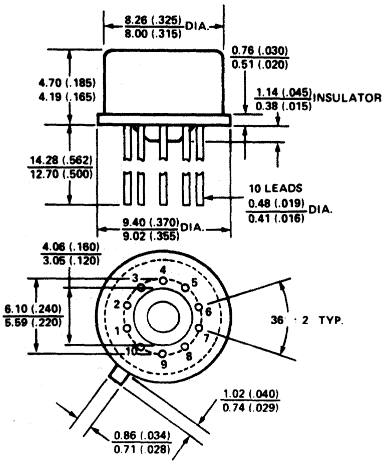
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

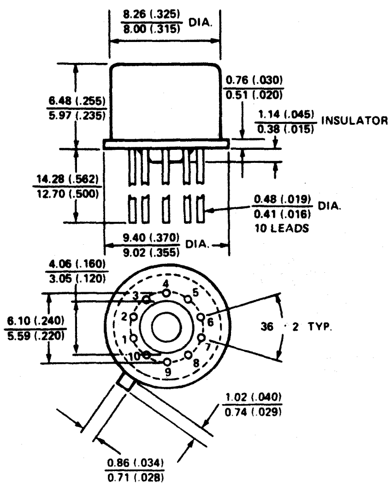
H PACKAGE — HERMETIC 8-PIN (TO-5 HEADER)



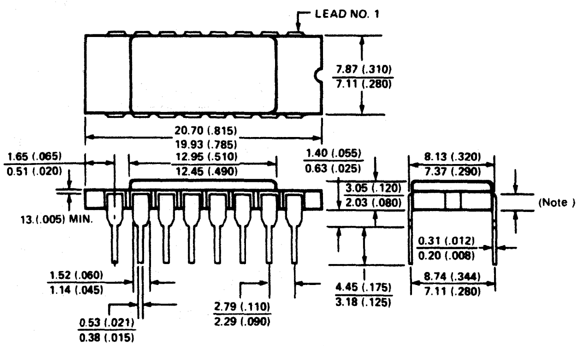
H PACKAGE — HERMETIC 10-PIN (TO-5/100 HEADER SHORT CAN)



H PACKAGE HERMETIC 10-PIN (TO-5/100 HEADER TALL CAN)



I PACKAGE — HERMETIC (16-PIN)



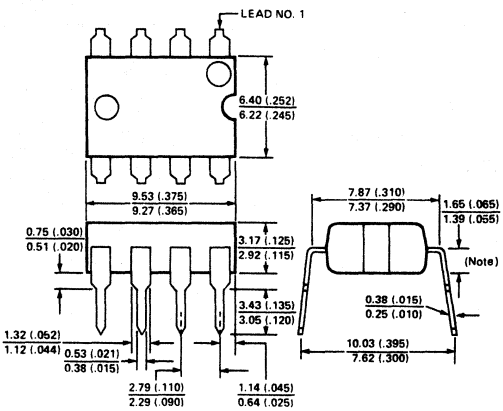
Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

9

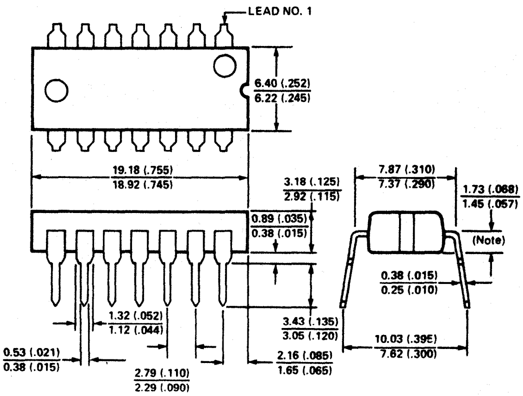
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

N PACKAGE — PLASTIC (8-PIN)



N PACKAGE — PLASTIC (14-PIN)

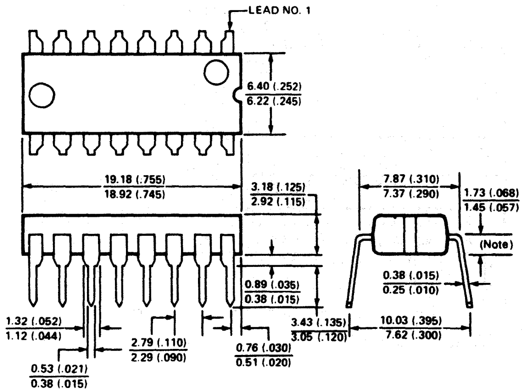


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

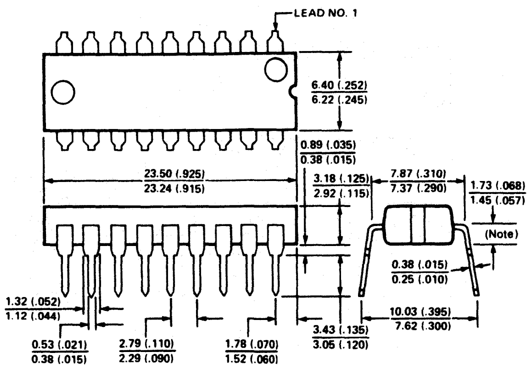
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

N PACKAGE — PLASTIC
(16-PIN)



N PACKAGE — PLASTIC
(18-PIN)

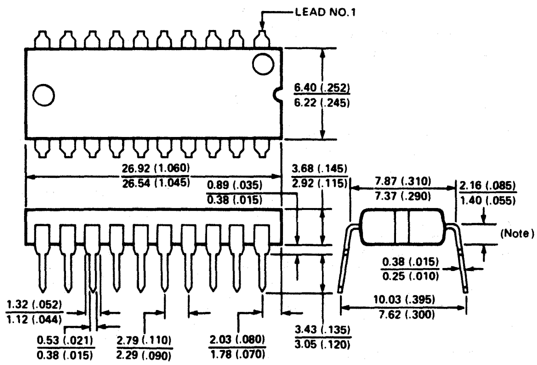


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

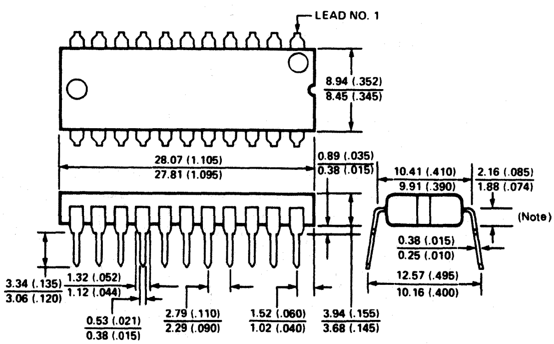
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

N PACKAGE — PLASTIC
(20-PIN)



N PACKAGE — PLASTIC
(22-PIN)

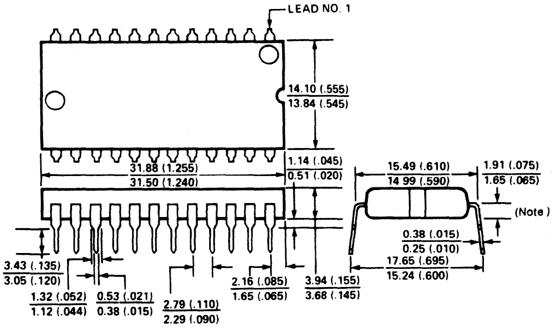


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

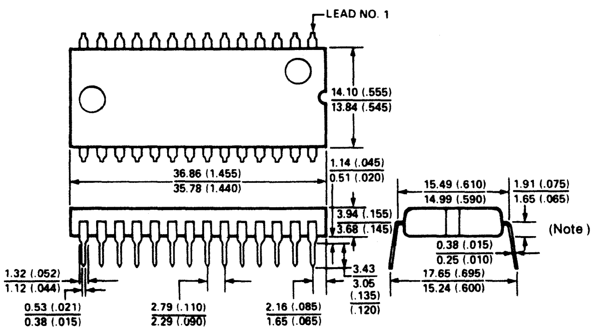
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

N PACKAGE — PLASTIC
(24-PIN)



N PACKAGE — PLASTIC
(28-PIN)



Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

9

PACKAGE OUTLINES

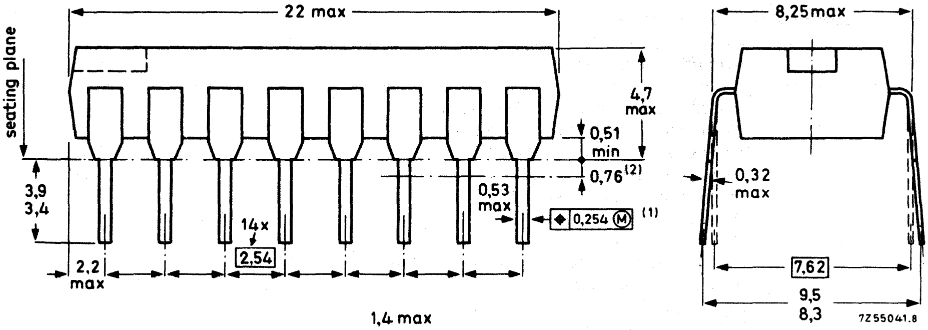
For prefixes: SAA, TCA, TDA, TDB, TEA

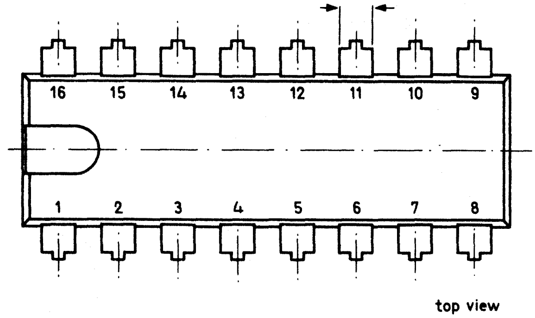
Introduction

The package information for each type number is given below:

type number	description and package code	page
SAA1027	16-lead dual in-line; plastic (SOT-38A)	9-19
SAA1029	16-lead dual in-line; plastic (SOT-38)	9-18
TCA520B	8-lead dual in-line; plastic (SOT-97A)	9-23
TCA520D	8-lead mini-pack; plastic (SO-8; SOT-96A)	9-22
TDA1023	16-lead dual in-line; plastic (SOT-38)	9-18
TDA1060	16-lead dual in-line; plastic (SOT-38)	9-18
TDA1060A	16-lead dual in-line; plastic (SOT-38)	9-18
TDA1060B	16-lead dual in-line; ceramic (cerdip) (SOT-74A, B, C)	9-21
TDA1060T	16-lead mini-pack; plastic (SO-16; SOT-109A)	9-25
TDB1080	16-lead dual in-line; plastic (SOT-38WE-2)	9-20
TDB1080T	16-lead mini-pack; plastic (SO-16; SOT-109A)	9-25
TEA1017	18-lead dual in-line; plastic (SOT-102CS, HE, KE, ME)	9-24
TEA1039	9-lead single in-line; plastic (SOT-110B)	9-26

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

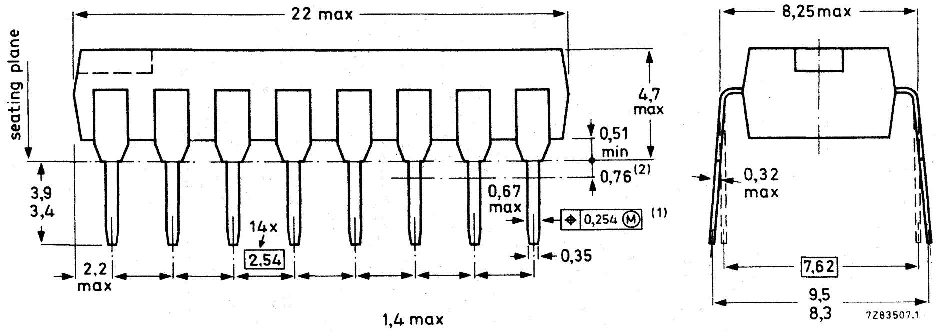
2. By dip or wave

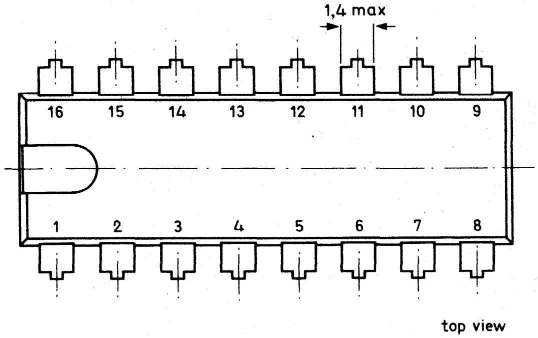
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38A)





⊕ Positional accuracy.

(M) Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

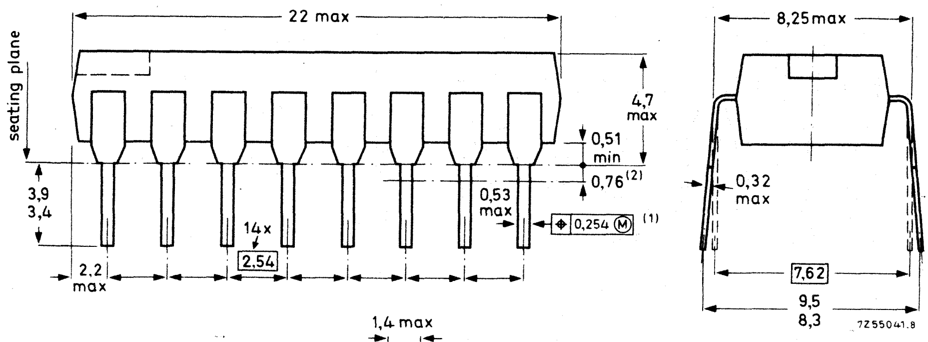
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

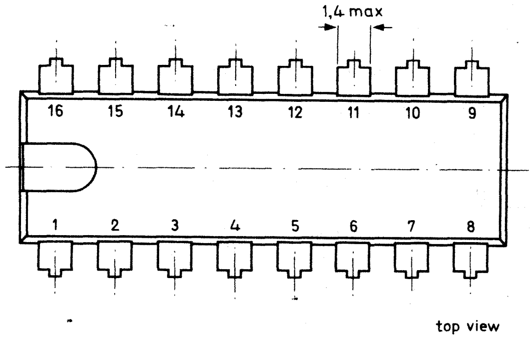
3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

9

16-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT-38WE-2)





⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 ^{o}C it must not be in contact for more than 10 seconds; if between 300 ^{o}C and 400 ^{o}C, for not more than 5 seconds.

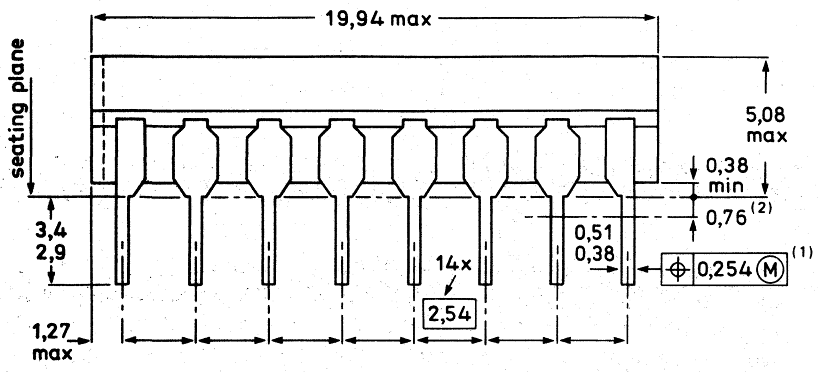
2. By dip or wave

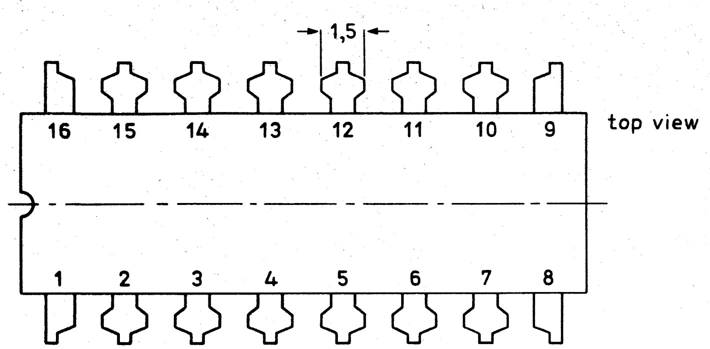
The maximum permissible temperature of the solder is 260 ^{o}C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

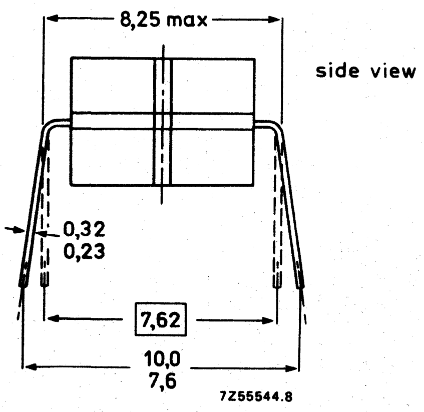
3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-74A,B,C)







⊕ Positional accuracy.

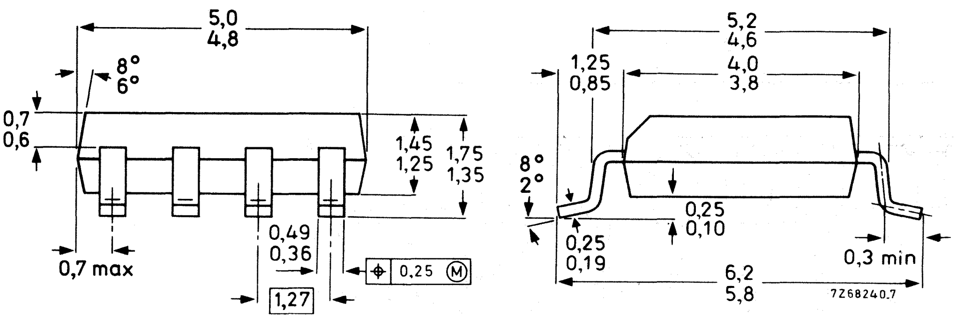
Ⓜ Maximum Material Condition.

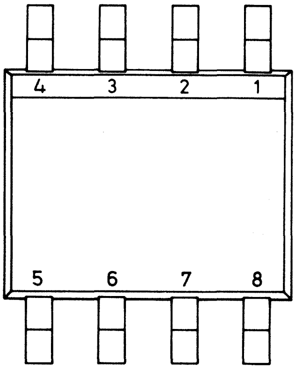
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO-8; SOT-96A)





top view

Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

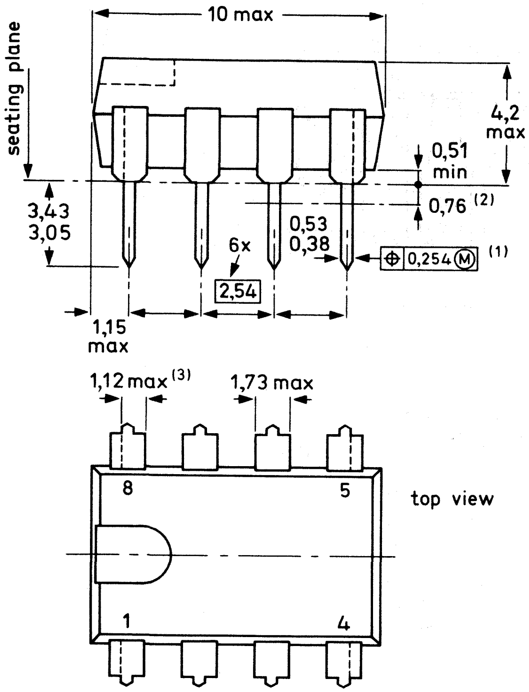
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

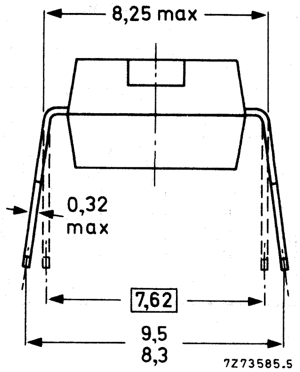
For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

8-LEAD DUAL IN-LINE; PLASTIC (SOT-97A)



top view



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

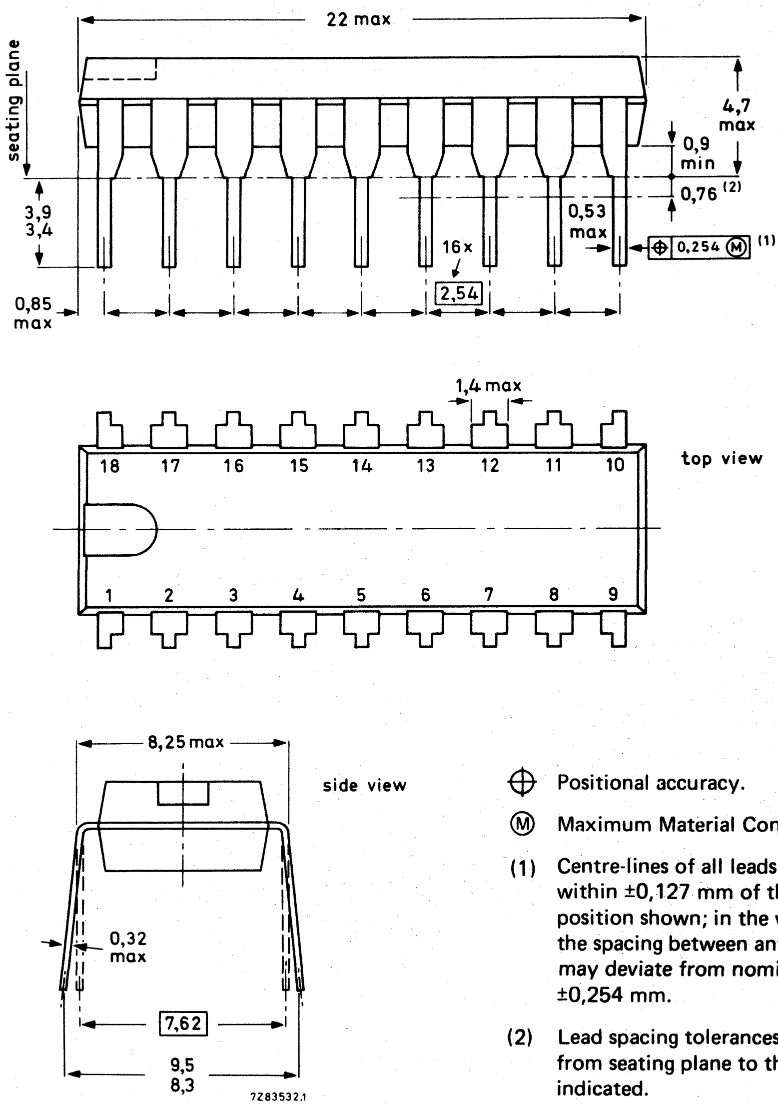
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102CS,HE,KE,ME)



⊕ Positional accuracy.

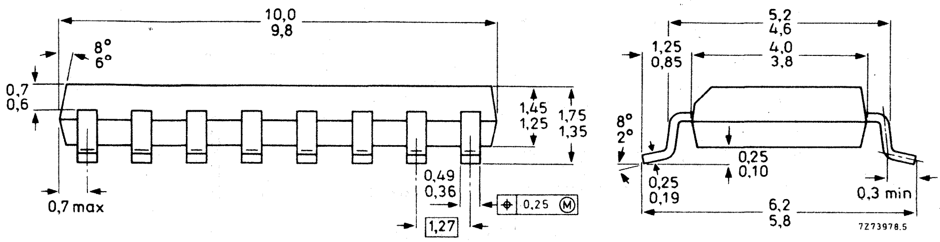
Ⓜ Maximum Material Condition.

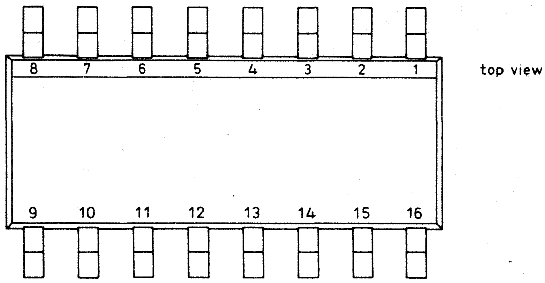
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO-16; SOT-109A)





Dimensions in mm

⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

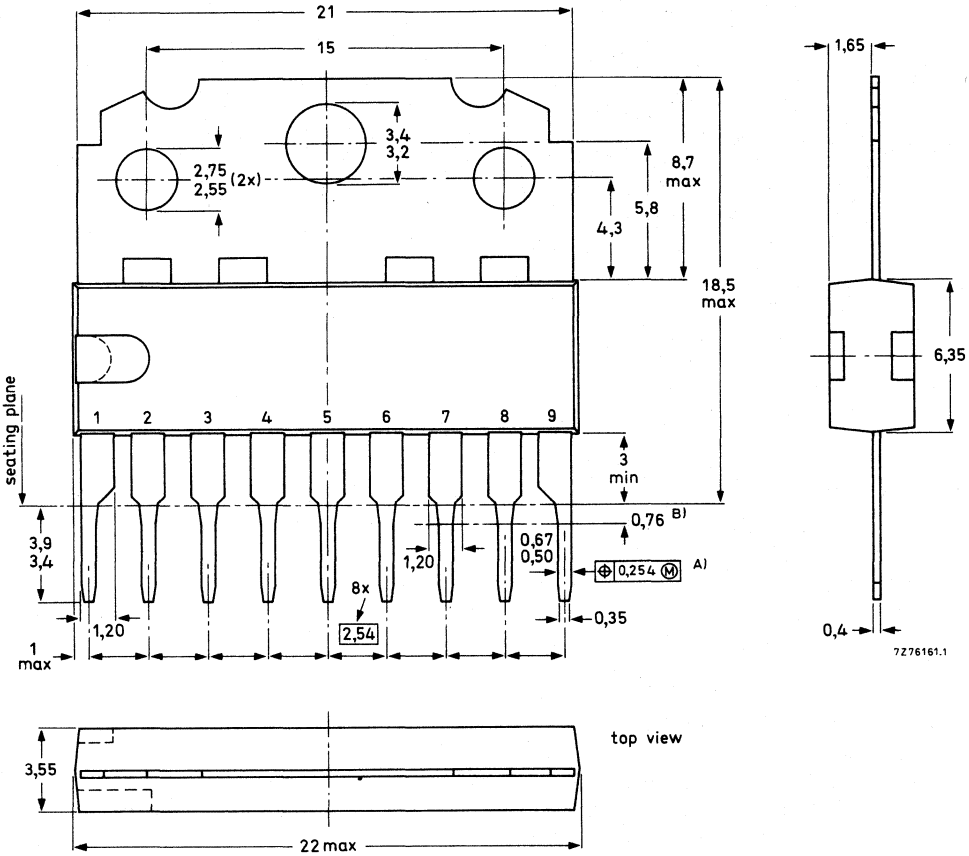
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110B)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

Section 10
Forthcoming New Products and Alphanumeric Index

INDEX

SECTION 10 – FORTHCOMING NEW PRODUCTS AND ALPHANUMERIC INDEX

FORTHCOMING NEW PRODUCTS BY PRODUCT GROUP

Amplifiers

NE5260	Voltage controlled amplifier
NE5212	Fiber optic preamplifier

Communications

NE568	150 MHz phase locked loop
NE575	Low voltage compandor
NE5050	Power line modem
MC3361	FM IC processor

Interface/Data Conversion

ADC0820	8-bit high speed CMOS A/D converter
NE5060	12-bit accuracy sample and hold amplifier
NE5082	Ethernet transceiver for local area network
NE5105	12-bit accuracy comparator

Power Conversion and Control

SG1524C/2524C/3524C	SMPS
SG1525/2525/3525	SMPS
SG1527/2527/3527	SMPS
SE/NE5563	SMPS – Improved NE5560

ALPHANUMERIC INDEX

Electronic components and materials for professional, industrial and consumer uses from the world-wide Philips Group of Companies

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Indonesia: P.T. PHILIPS-RALIN ELECTRONICS, Elcoma Div., Setiabudi II Building, 6th Fl., Jalan H.R. Rasuna Said (P.O. Box 223/KBY) Kuningan,
JAKARTA – Selatan, Tel. 512572.
Ireland: PHILIPS ELECTRICAL (IRELAND) LTD., Newstead, Clonskeagh, DUBLIN 14, Tel. 693355.
Italy: PHILIPS S.p.A., Sezione Elcoma, Piazza IV Novembre 3, I-20124 MILANO, Tel. 2-6752.1.
Japan: NIHON PHILIPS CORP., Shuwa Shinagawa Bldg., 26-33 Takanawa 3-chome, Minato-ku, TOKYO (108), Tel. 448-5611.
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